EE 330
Lecture 19

Guest Speaker: David Ripley of Skyworks

Bipolar Device Operation and Modeling

Guest Speaker: David Ripley

BS	EE	ISU	1992
MS	EE	National Technical University	2002

Motorola	Design and Development	TDMA and Amplifies	1992-1999
Skyworks Solutions (Conexant)	Senior Technical Director		1999-Present

Currently holds 150 patents

A Single Chip HBT Power Amplifier with Integrated Power Control

David Ripley – Skyworks Solutions, Inc.

RTU2B-1

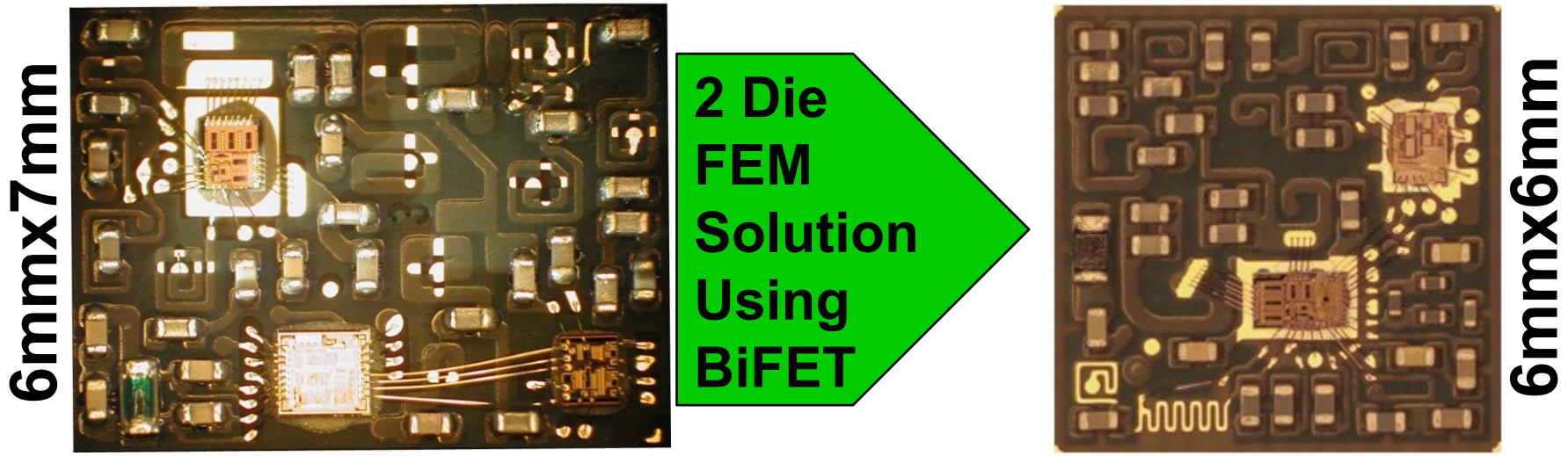
SKYWORKS®
BREAKTHROUGH SIMPLICITY

Outline

- Goals for this work
- Solution Block Diagram
- Circuit Schematic Details
- Device Layout
- Measured Performance
- Summary

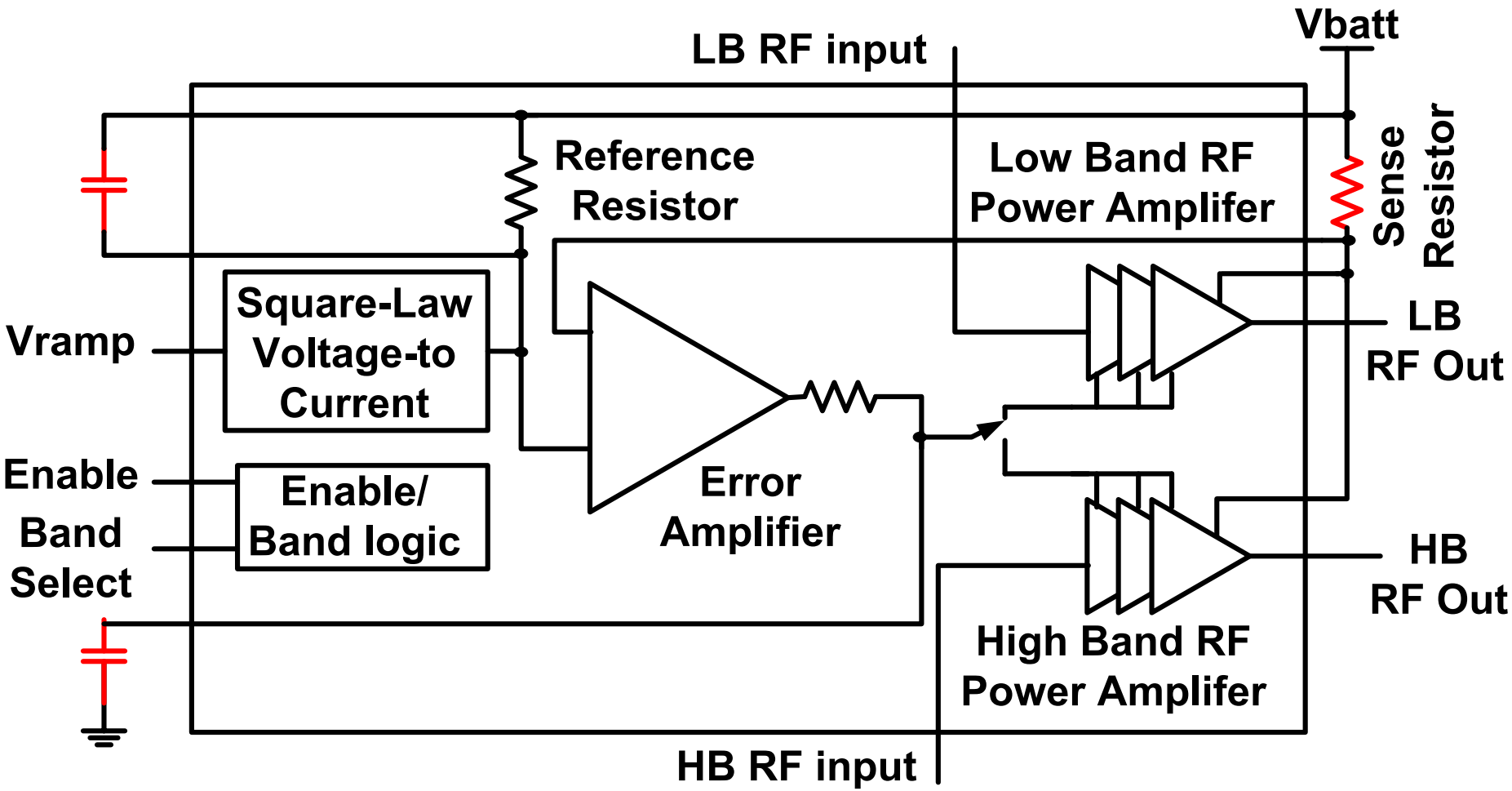
Introduction

- Goal:
  - Develop a 2G PA solution maintaining the RF performance of HBT while delivering next generation size and cost



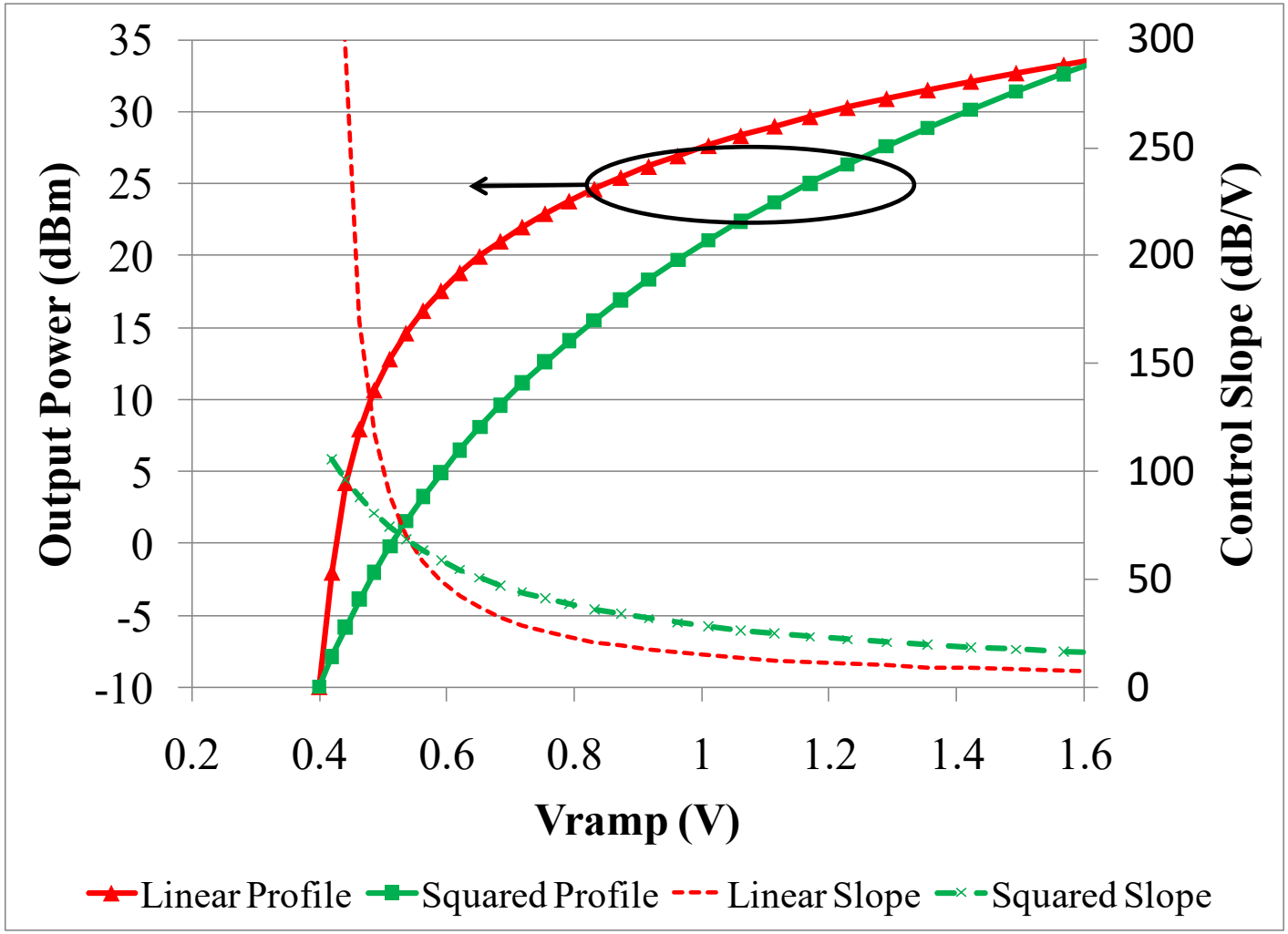
Reduce Size and Cost Through Die Elimination

Power Control Block Diagram



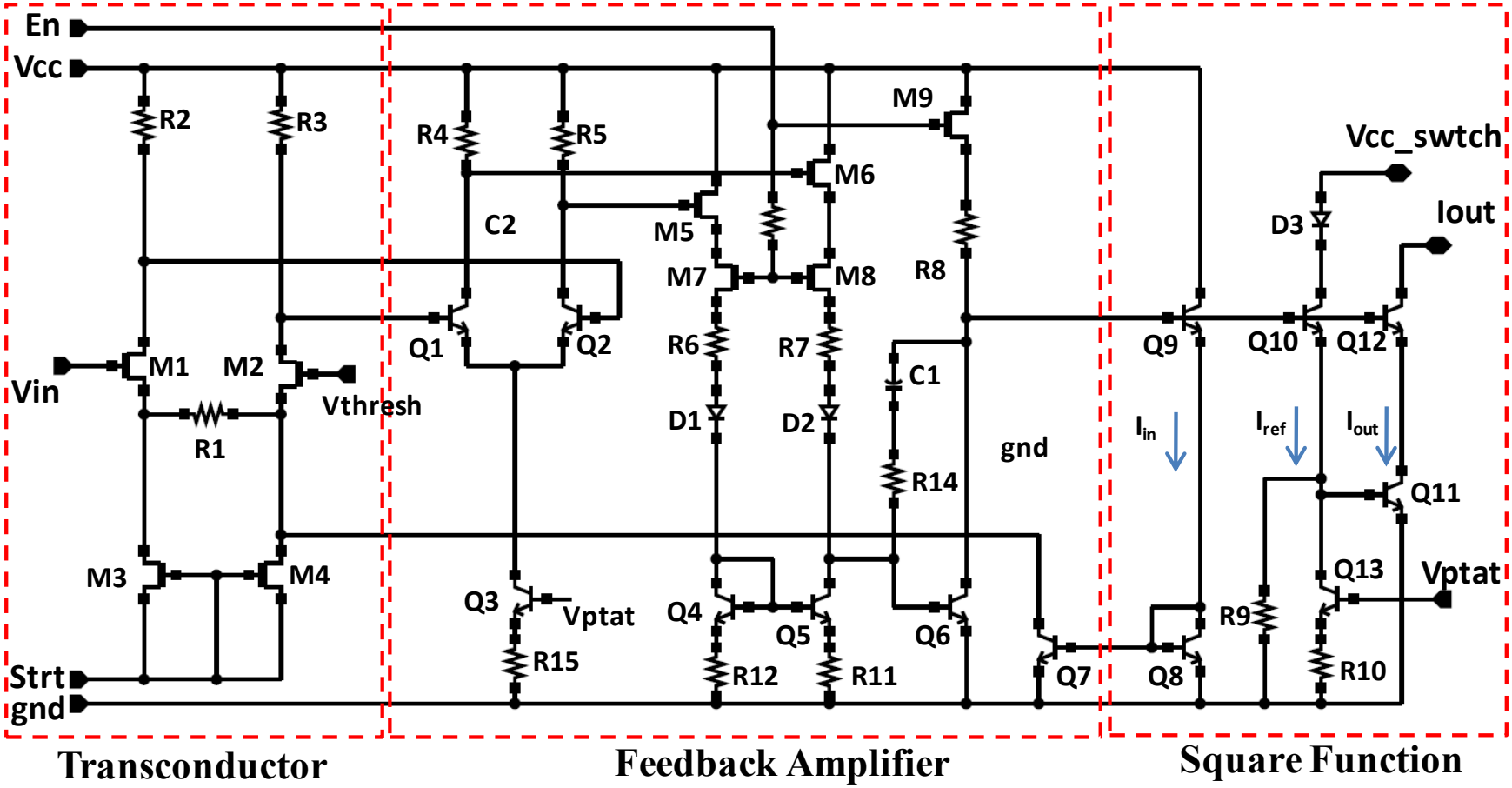
Indirect control of RF power through DC current

Importance of Squaring Response



~3x improvement in control slope

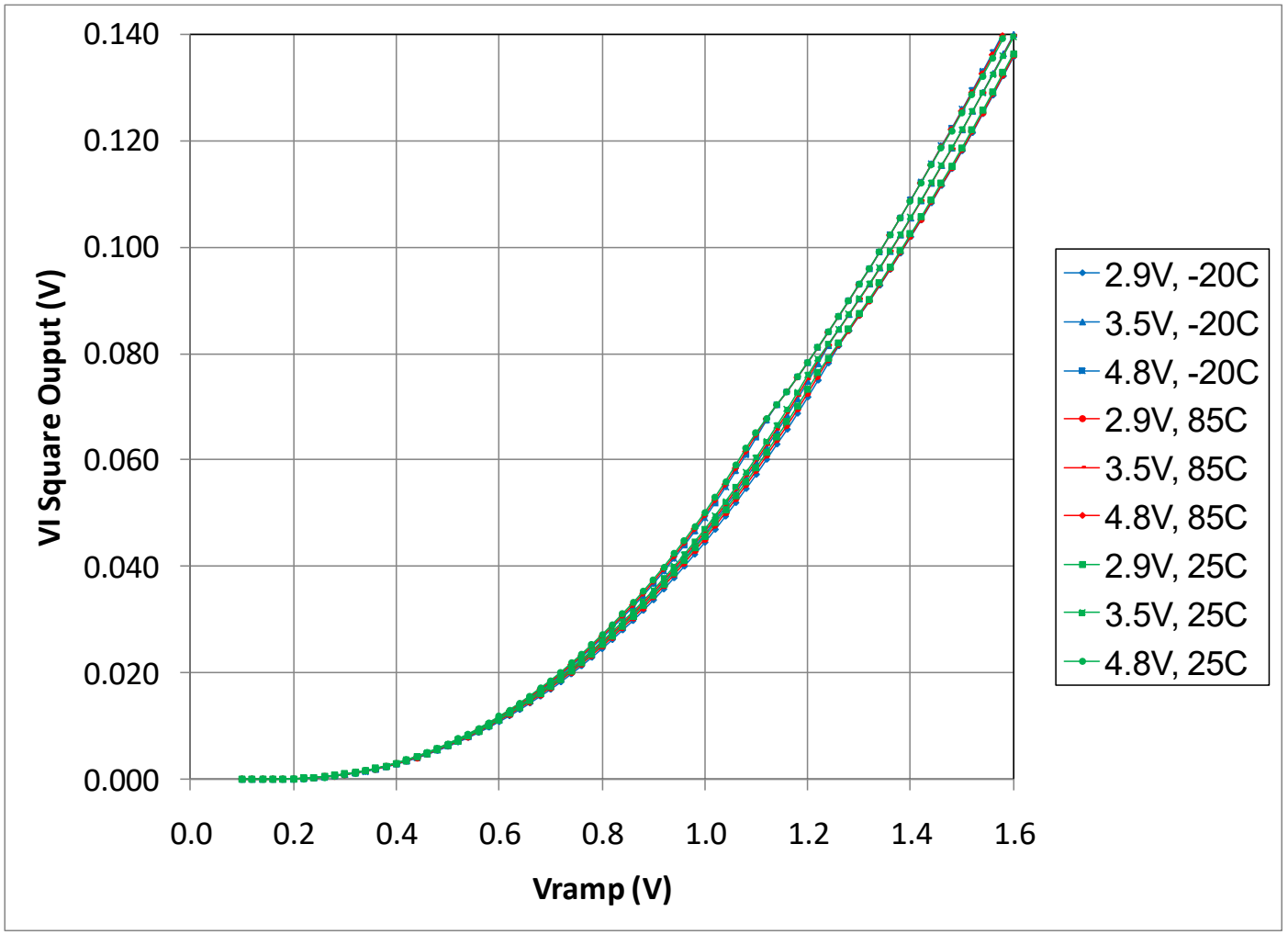
Voltage-to-Current Processing



$$I_{in} = (V_{in} - V_{thresh})/R_1 \qquad I_{out} = I_{in}^2/I_{ref}$$

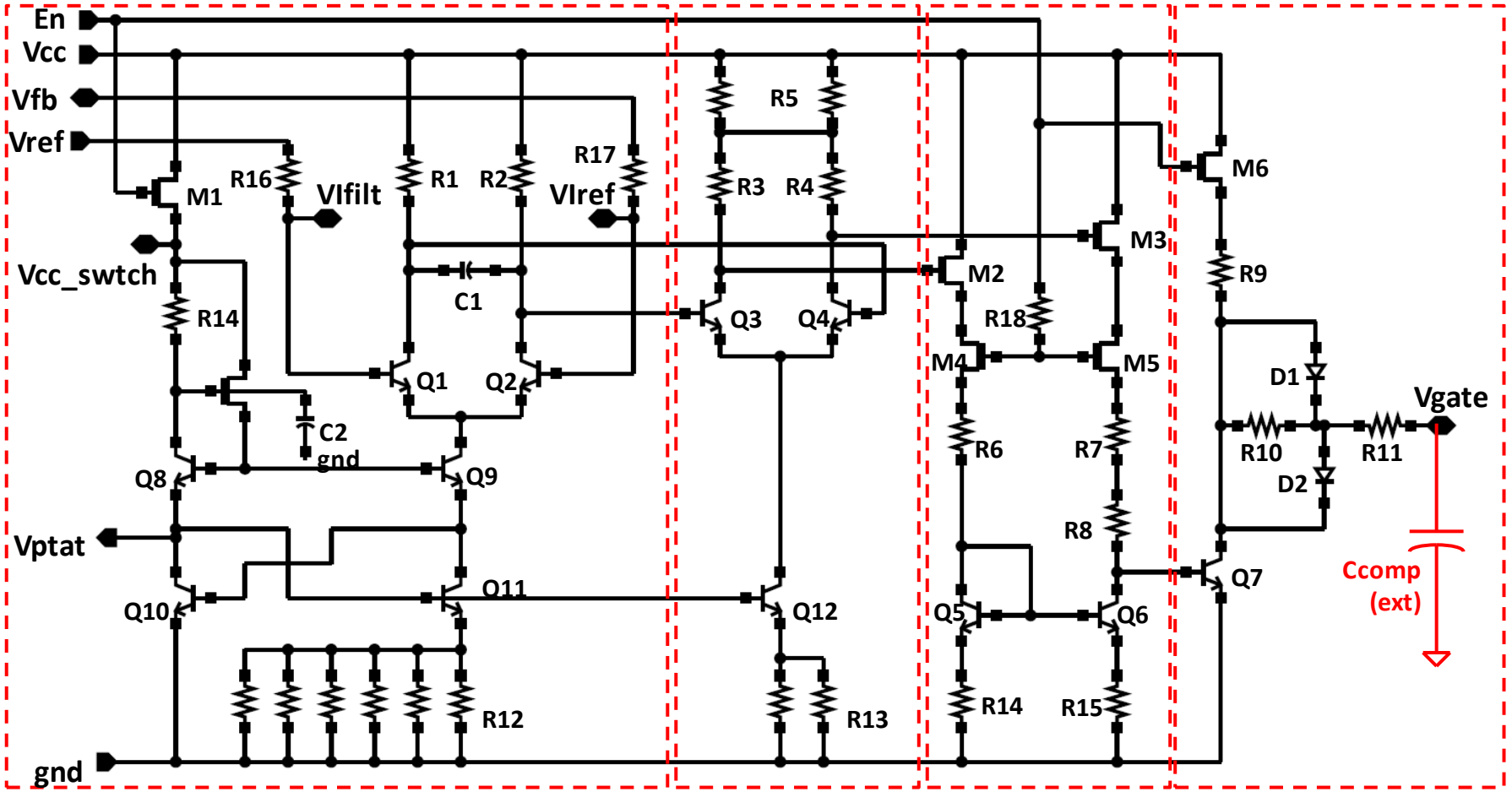
CMOS Compatible Interface with low dB/V control

Square Function Response



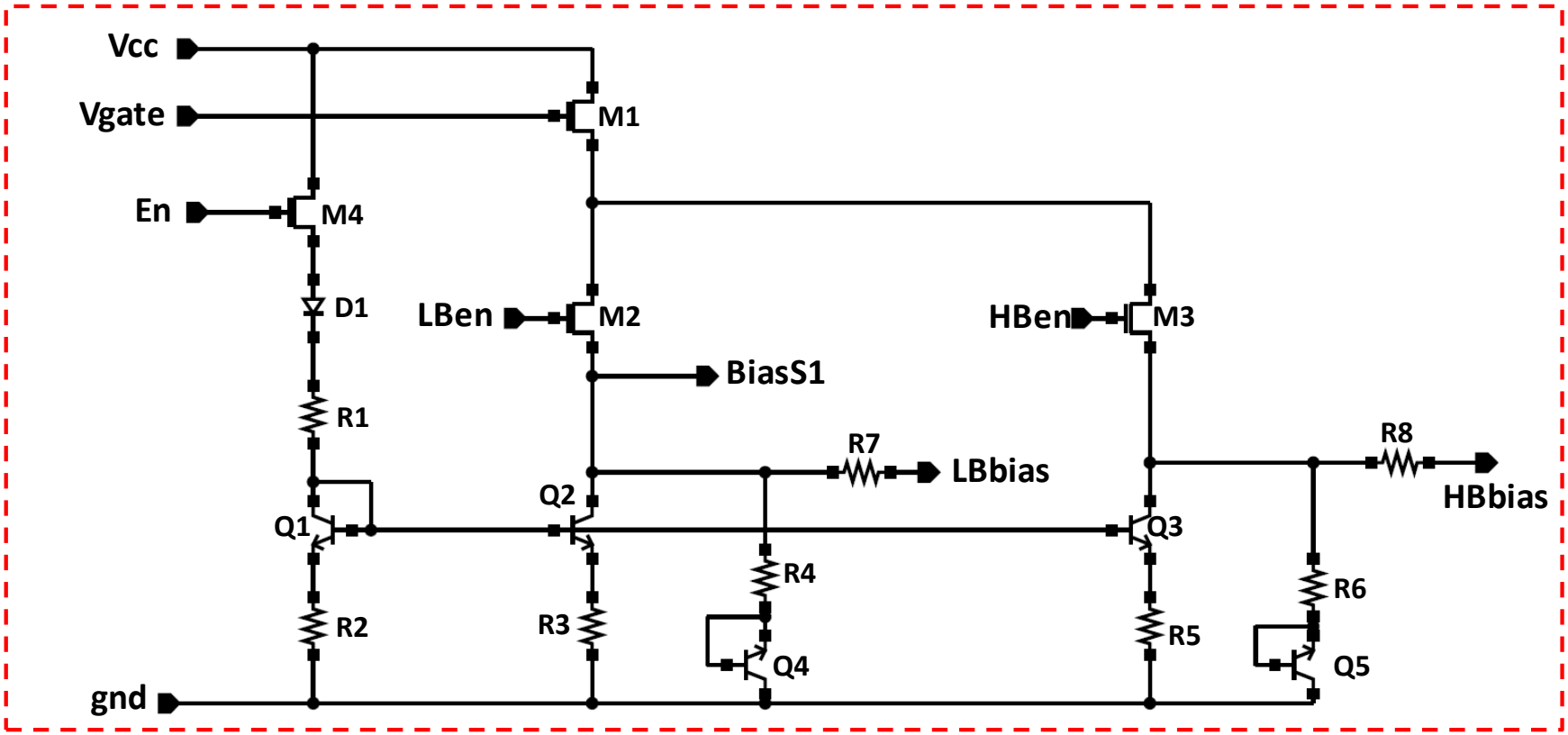
Process, Temperature, Supply insensitive design

Core Bias and Error Amplifier



Precision Design for Offset, Transient and Noise

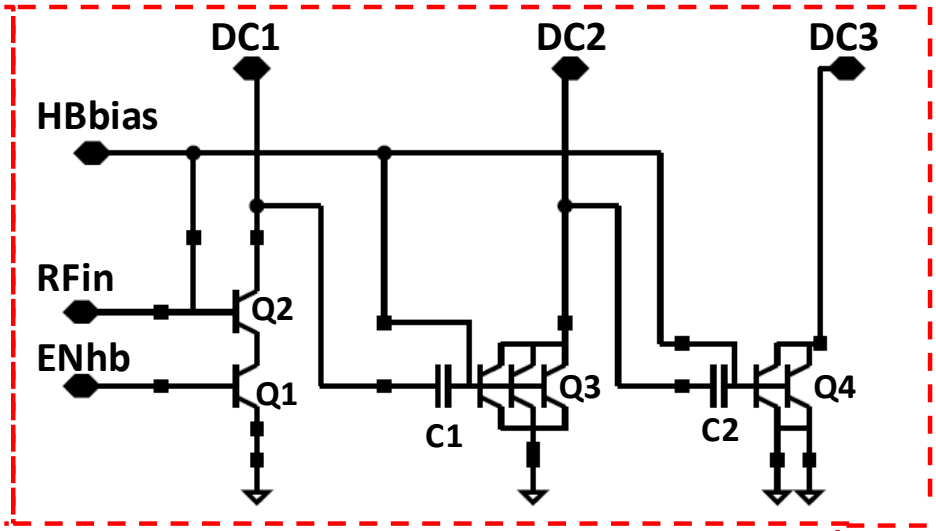
PA Bias Interface



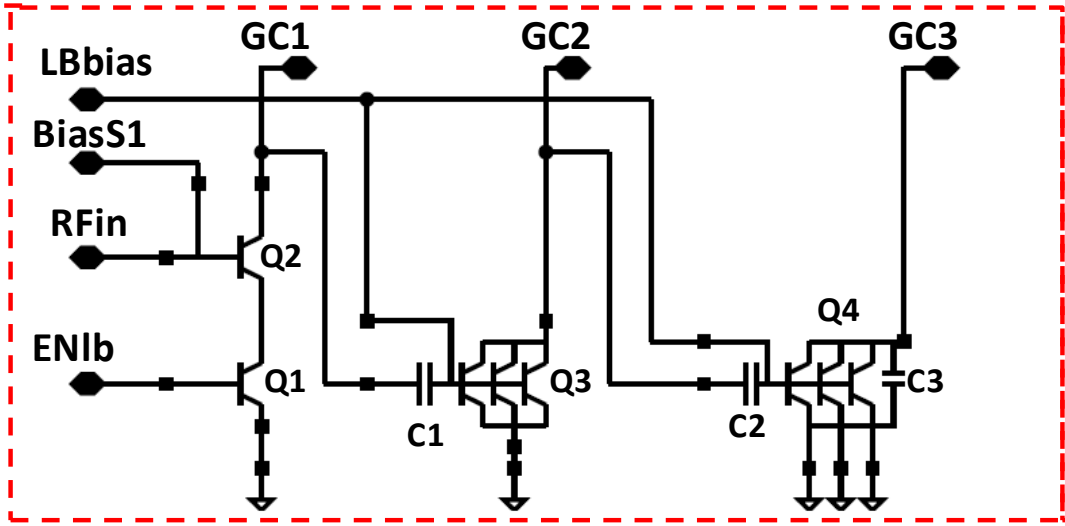
RF Power Amplifier Bias interface

Single Follower Switched for Dual Band Support

Power Amplifier



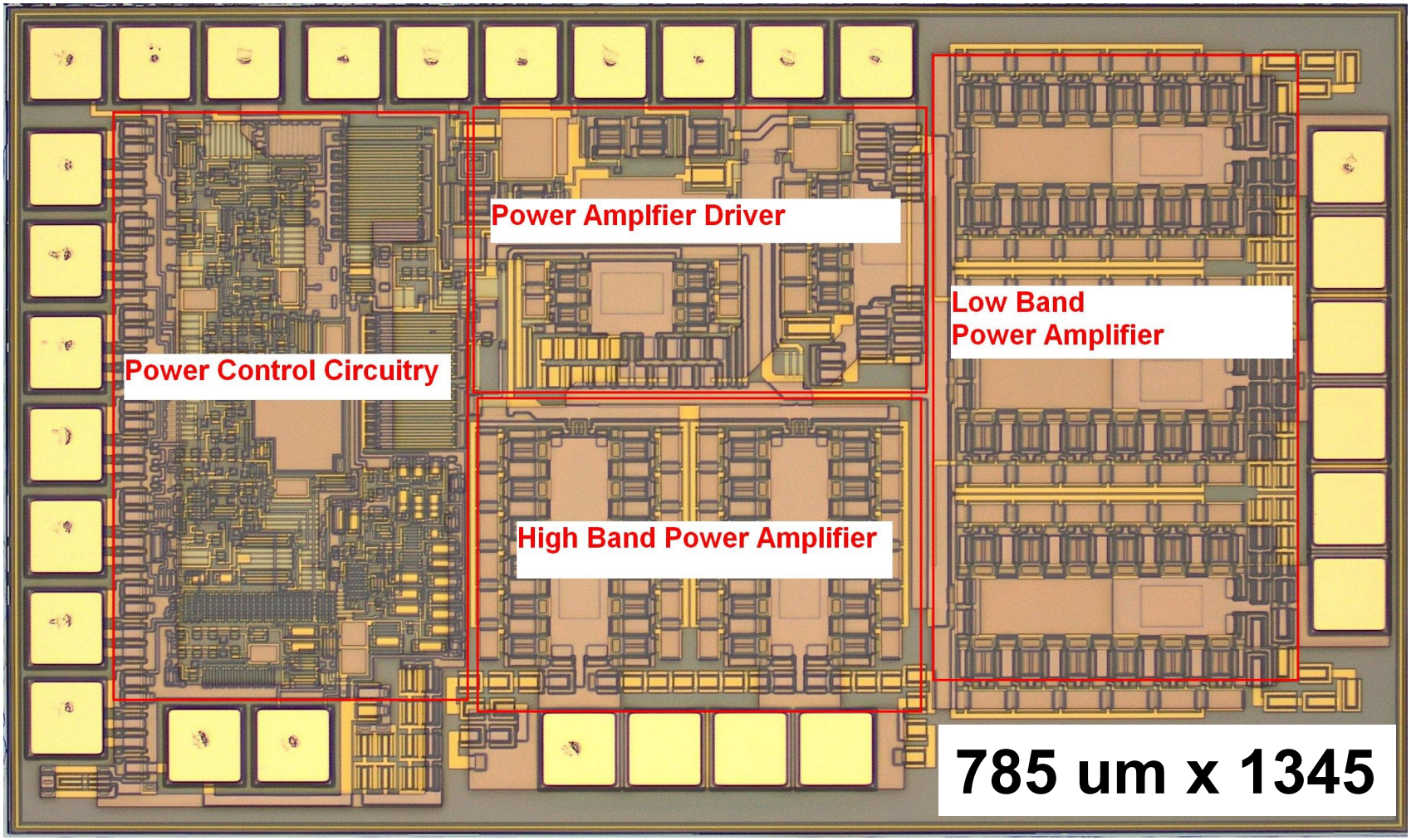
High Band RF Power Amplifier



Low Band RF Power Amplifier

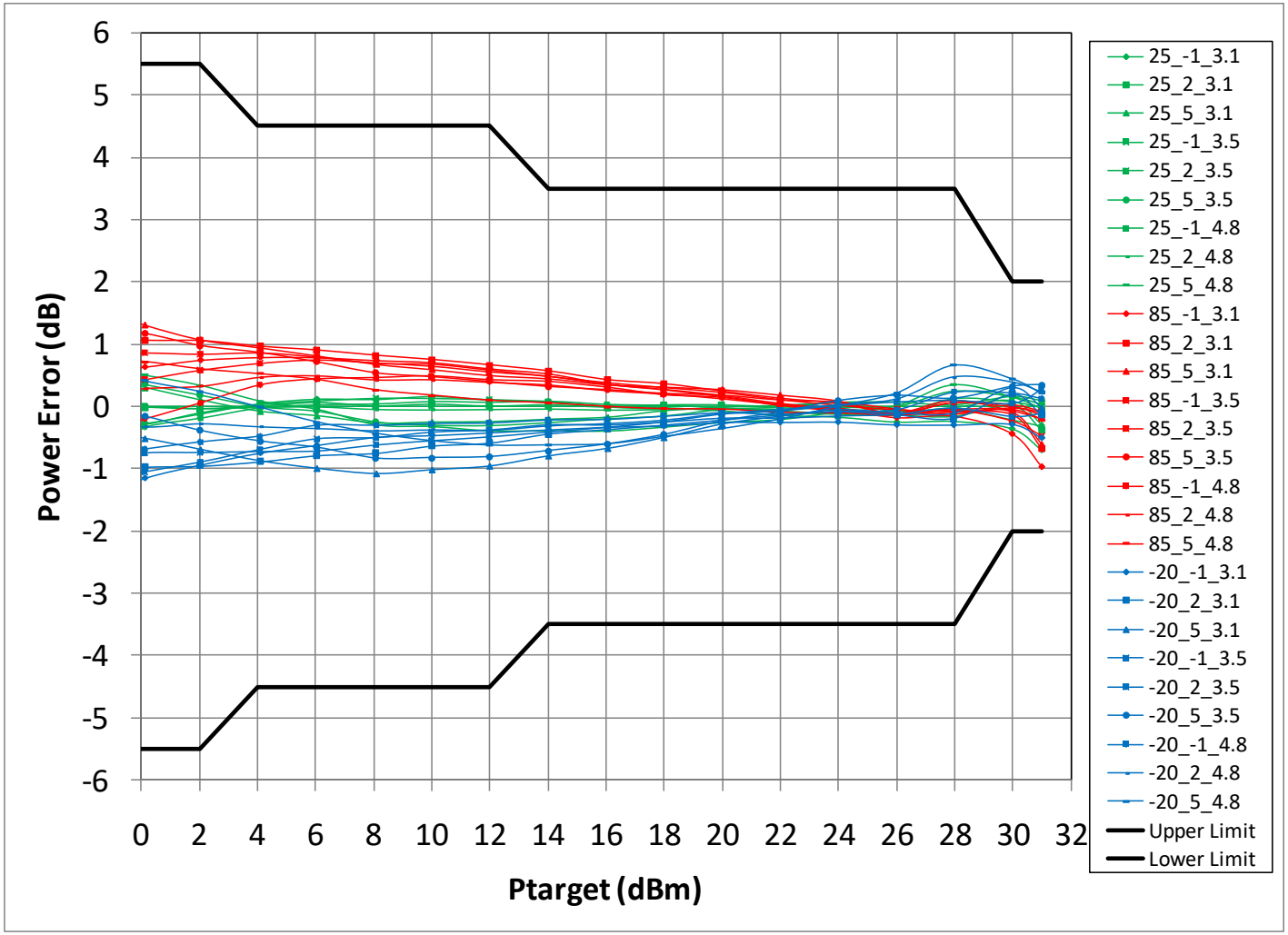
Q1 Supports High Forward Isolation Performance

Complete HBT Die



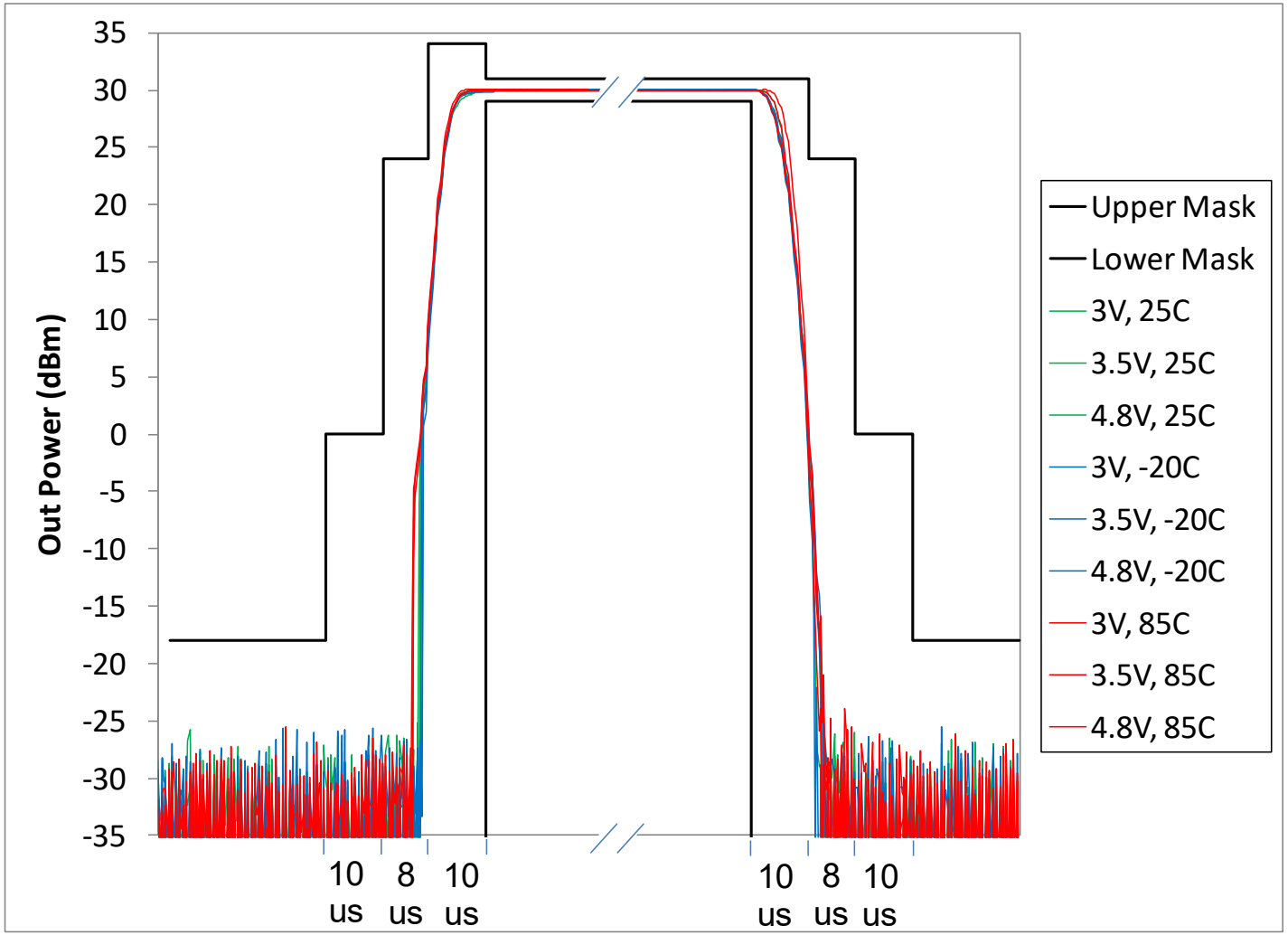
Power Amplifier with Integrated Control

Module Power Control Accuracy



Significant Margin to 3GPP Standard

Burst Time Mask Performance



Transient satisfies time and spectral masks

Summary

- BiFET HBT technology enables integration of PA and control on a single die
- Circuit solutions were developed to meet all 3GPP systems standards with margin
- Detailed Device simulations are confirmed through extensive testing and through sustained high volume production

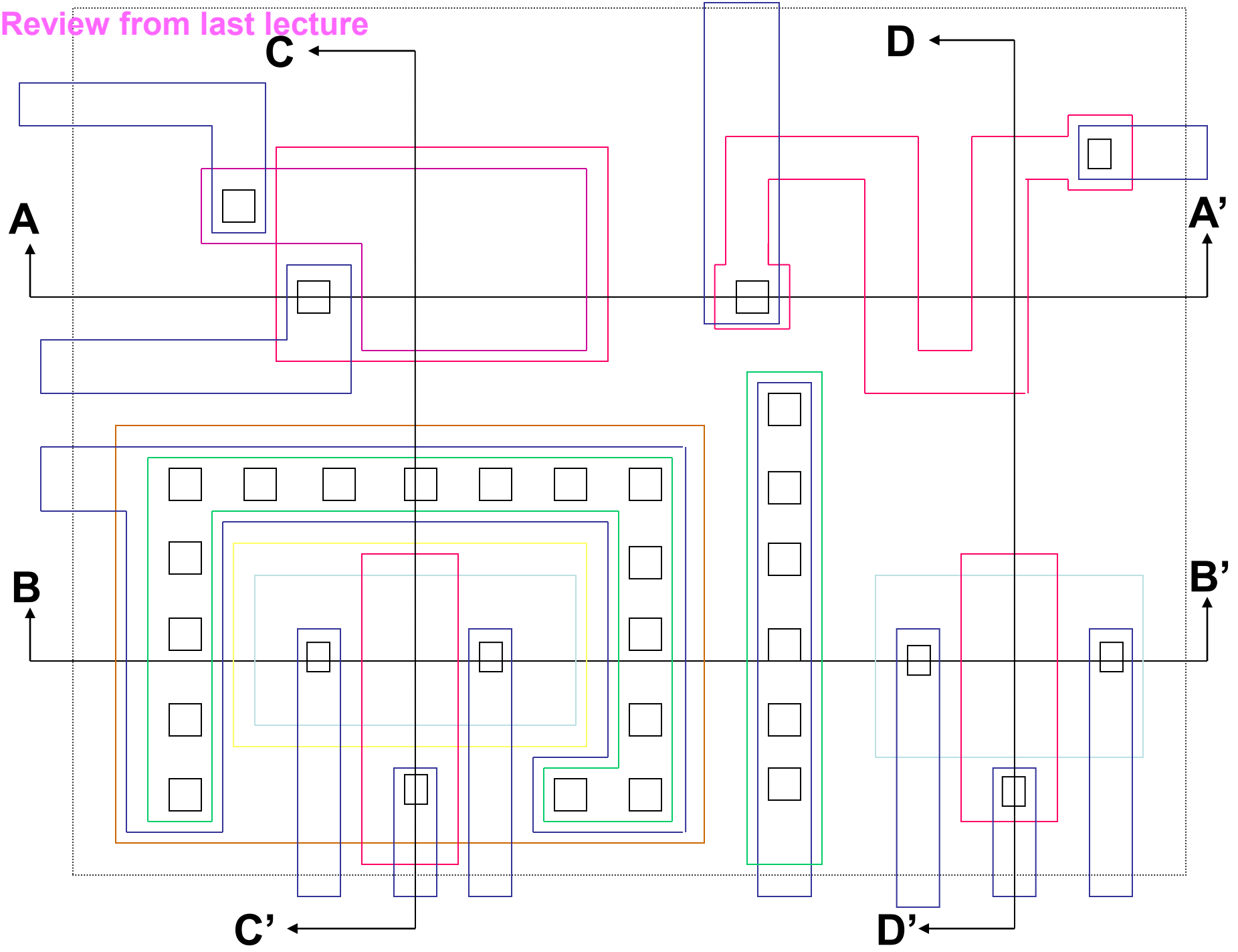
Thanks to Hongxiao Shao for PDK development,
Pete Zampardi for process and modeling,
Phil Lehtola for RF PA and module design,
Robert Rammelsberg for design verification.

Review from last lecture

TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process[a]

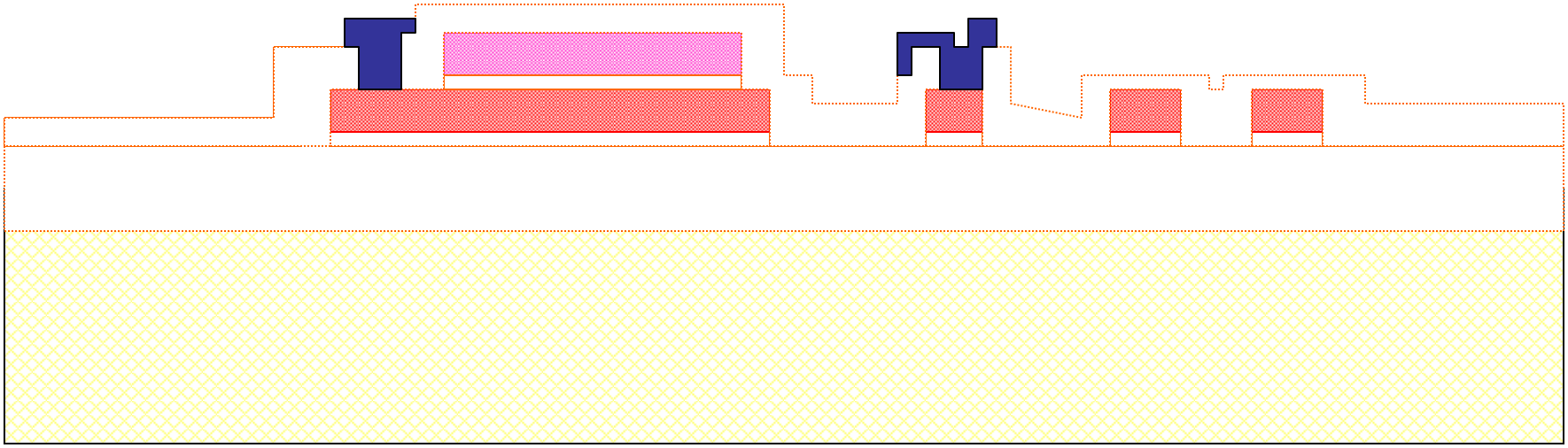
1.	Clean wafer	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN **n-well**	(MASK #1)
5.	Develop photoresist	
6.	Deposit and diffus n-type impurities	
7.	Strip photoresist	
8.	Strip thin oxide	
9.	Grow thin oxide	
10.	Apply layer of Si_3N_4	
11.	Apply photoresist	
12.	PATTERN Si_3N_4 (active area definition)	(MASK #2)
13.	Develop photoresist	
14.	Etch Si_3N_4	
15.	Strip photoresist	
	Optional field threshold voltage adjust	
	A.1 Apply photoresist	
	A.2 PATTERN ANTIMOAT IN SUBSTRATE	(MASK #A1)
	A.3 Develop photoresist	
	A.4 FIELD IMPLANT p-type)	
	A.5 Strip photoresist	
16.	GROW FIELD OXIDE	
17.	Strip Si_3N_4	
18.	Strip thin oxide	
19.	GROW GATE OXIDE	
20.	POLYSILICON DEPOSITION (POLY I)	
21.	Apply photoresist	
22.	PATTERN POLYSILICON	(MASK #3)
23.	Develop photoresist	
24.	ETCH POLYSILICON	

Review from last lecture

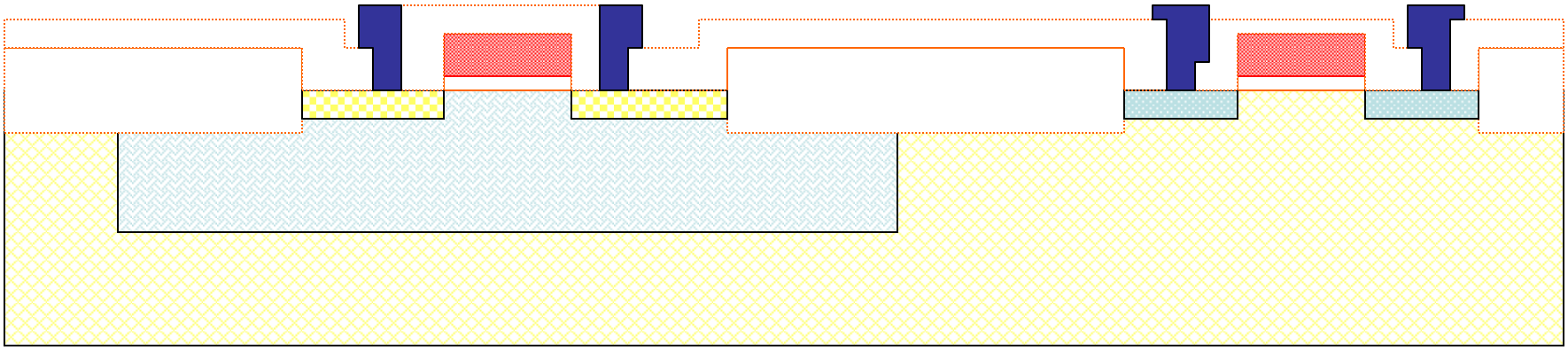


Review from last lecture

Metal Mask



A-A' Section



B-B' Section

Should now know what you can do in this process !!

Can metal connect to active?

Can metal connect to substrate when on top of field oxide?

How can metal be connected to substrate?

Can poly be connected to active under gate?

Can poly be connected to active any place?

Can metal be placed under poly to isolate it from bulk?

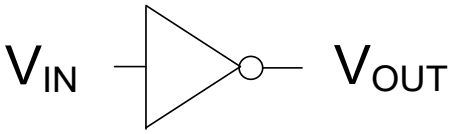
Can metal 2 be connected directly to active?

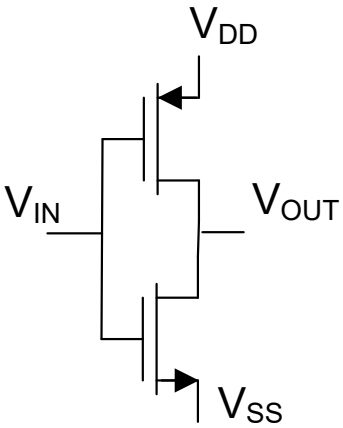
Can metal 2 be connected to metal 1?

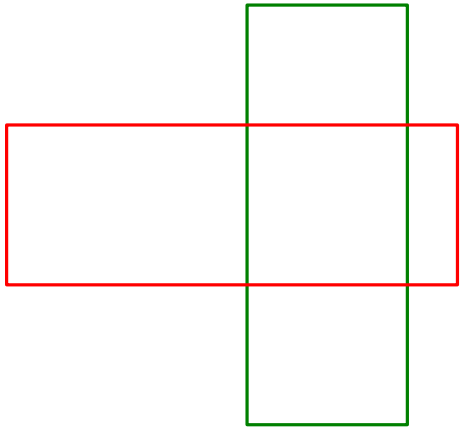
Can metal 2 pass under metal 1?

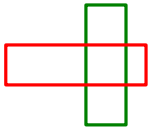
Could a process be created that will result in an answer of YES to most of above?

How does the minimum-sized inverter delay when driving an identical device compare between a 0.5u process and a 0.18u process?

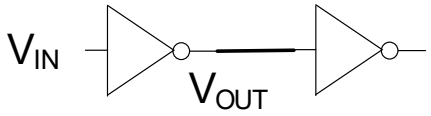




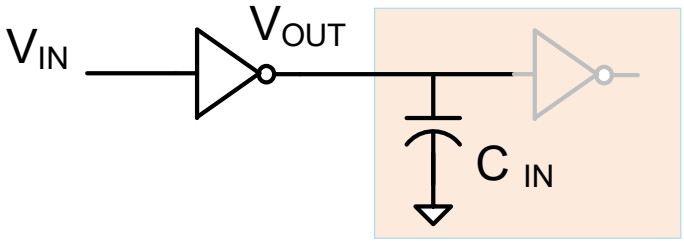




How does the minimum-sized inverter delay when driving an identical device compare between a 0.5u process and a 0.18u process?



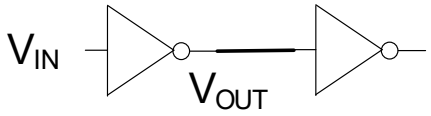
Recall:



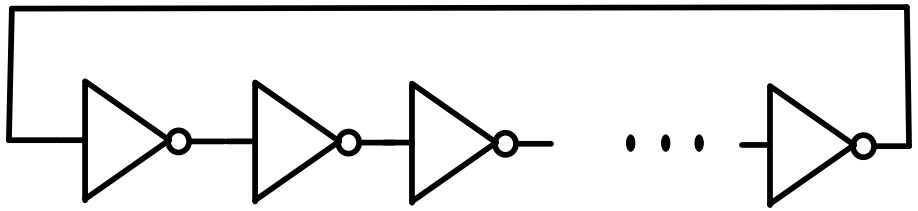
$$C_{IN}=C_{GSn}+C_{GSp}$$

$$t_{HL}=R_{PD}C_{IN}$$
$$t_{LH}=R_{PU}C_{IN}$$
$$t_{PROP}=t_{HL}+t_{LH}$$

How does the minimum-sized inverter delay when driving an identical device compare between a 0.5u process and a 0.18u process?



It will also be shown later that if n inverters are connected in a loop and if n is odd, this will form a “ring” oscillator:



$$f_{OSC} \cong \frac{1}{nt_{PROP}}$$

RUN: T91T
VENDOR: AMIS
TECHNOLOGY: SCN05
FEATURE SIZE: 0.5 microns
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.81	-0.92	volts
SHORT	20.0/0.6			
Idss		466	-250	uA/um
Vth		0.69	-0.89	volts
Vpt		12.7	-11.7	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	20.0/20.0			
Vth		0.71	-0.94	volts
Vjbkd		8.8	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.44	0.57	V^0.5
K' (Uo*Cox/2)		54.8	-19.7	uA/V^2
Low-field Mobility		434.84	156.32	cm^2/V*s

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	M1	UNITS
Sheet Resistance	85.3	111.2	22.4	1033	0.09	ohms/sq
Contact Resistance	59.6	145.4	17.9			ohms
Gate Oxide Thickness	137					angstroms

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	UNITS
Area (substrate)	443	745	102			aF/um^2
Area (N+active)			2518			aF/um^2
Area (P+active)			2441			aF/um^2
Area (poly)				896	61	aF/um^2

CIRCUIT PARAMETERS		UNITS
Ring Oscillator Freq.		
DIV256 (31-stg,5.0V)	94.47	MHz
Ring Oscillator Power		
DIV256 (31-stg,5.0V)	0.48	uW/MHz/gate

MOSIS WAFER ACCEPTANCE TESTS

RUN: T4BK (MM_NON-EPI_THK-MTL) VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.53	volts
SHORT	20.0/0.18			
Idss		571	-266	uA/um
Vth		0.51	-0.53	volts
Vpt		4.7	-5.5	volts
WIDE	20.0/0.18			
Ids0		22.0	-5.6	pA/um
LARGE	50/50			
Vth		0.42	-0.41	volts
Vjbkd		3.1	-4.1	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		171.8	-36.3	uA/V^2
Low-field Mobility		398.02	84.10	cm^2/V*s

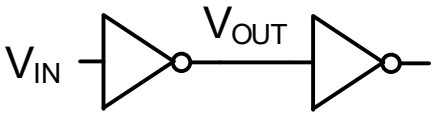
CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	998	1152	103	39	19	13	9	8	3		129		127	aF/um^2
Area (N+active)			8566	54	21	14	11	10	9					aF/um^2
Area (P+active)			8324											aF/um^2
Area (poly)				64	18	10	7	6	5					aF/um^2
Area (metal1)					44	16	10	7	5					aF/um^2
Area (metal2)						38	15	9	7					aF/um^2
Area (metal3)							40	15	9					aF/um^2
Area (metal4)								37	14					aF/um^2
Area (metal5)									36			1003		aF/um^2
Area (r well)	987													aF/um^2
Area (d well)										574				aF/um^2
Area (no well)	139													aF/um^2
Fringe (substrate)	244	201		18	61	55	43	25						aF/um
Fringe (poly)				69	39	29	24	21	19					aF/um
Fringe (metal1)					61	35		23	21					aF/um
Fringe (metal2)						54	37	27	24					aF/um
Fringe (metal3)							56	34	31					aF/um
Fringe (metal4)								58	40					aF/um
Fringe (metal5)									61					aF/um
Overlap (P+active)			652											aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.74	volts
Vinv	1.5	0.78	volts
Vol (100 uA)	2.0	0.08	volts
Voh (100 uA)	2.0	1.63	volts
Vinv	2.0	0.82	volts
Gain	2.0	-23.33	
Ring Oscillator Freq.			
D1024_THK (31-stg,3.3V)		338.22	MHz
DIV1024 (31-stg,1.8V)		402.84	MHz
Ring Oscillator Power			
D1024_THK (31-stg,3.3V)		0.07	uW/MHz/gate
DIV1024 (31-stg,1.8V)		0.02	uW/MHz/gate

How does the minimum-sized inverter delay compare between a 0.5u process and a 0.18u process?

Feature	0.5	0.18		Units
Vtn	0.81	0.5		V
Vtp	-0.92	-0.53		V
uCoxn	109.6	344		uA/V^2
uCoxp	39.4	72.6		uA/V^2
Cox	2.51	8.5		fF/µm^2
Vdd	5	1.8		V
fosc-31	94.5	402.8		MHz

Assume n-channel and p-channel devices with L=Lmin, W=1.5Lmin



$t_{HL}=R_{pd}C_L$

$t_{LH}=R_{pd}C_L$

$$R_{pd}=\frac{L_n}{\mu_n C_{OX} W_n (V_{DD}-V_{TN})}$$

$$R_{pu}=\frac{L_p}{\mu_p C_{OX} W_p (V_{DD}+V_{TP})}$$

$$C_L = C_{OX}\left(W_n L_n + W_p L_p\right)$$

Feature	0.5	0.18		Units
CL	1.88	0.83		fF
Rpd	1452	1491		ohms
Rpu	2858	3941		ohms
THL	2.73	1.23		psec
TLH	5.38	3.26		psec
f	123	223		GHz

Note 0.18u process is much faster than 0.5u process

Some scale even faster

Basic Devices and Device Models

- Resistor
- Diode
- Capacitor
- MOSFET
- BJT

Lets pick up a discussion of
Technology Files before moving to BJT

Return to basic devices !

Basic Devices and Device Models

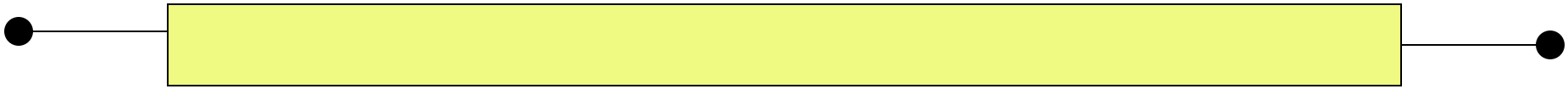
- Resistor
- Diode
- Capacitor
- MOSFET
- BJT

Bipolar Junction Transistors

- Operation
- Modeling

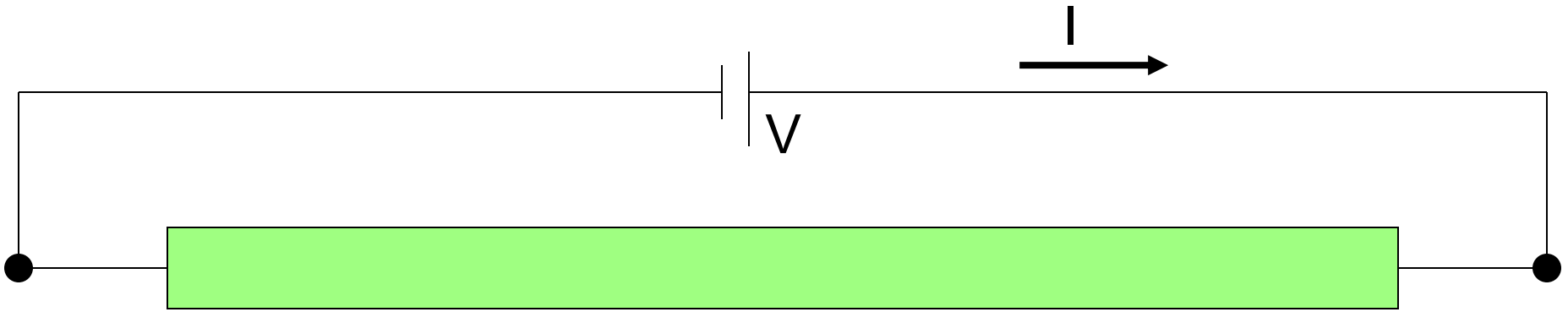
Carriers in Doped Semiconductors

n-type



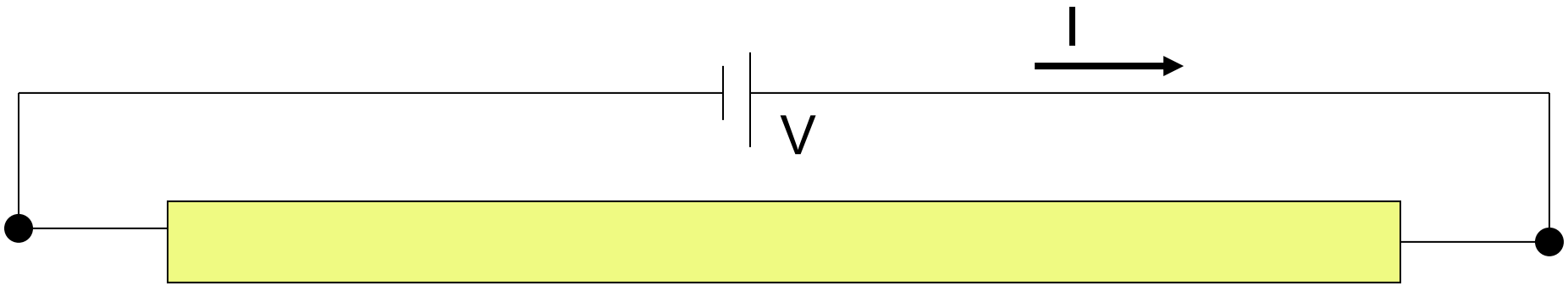
p-type

Carriers in Doped Semiconductors



Current carriers are dominantly electrons

Small number of holes are short-term carriers



Current carriers are dominantly holes

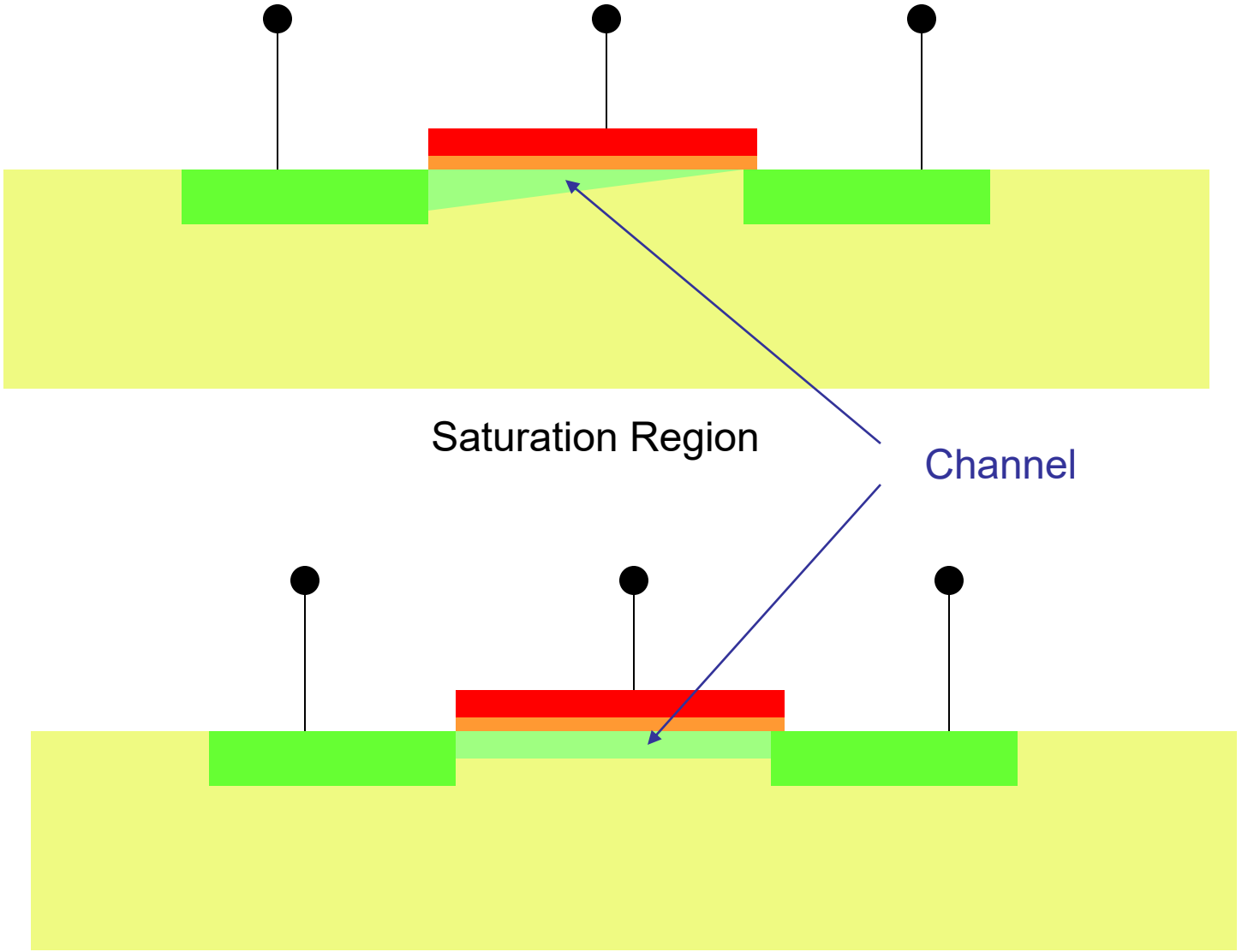
Small number of electrons are short-term carriers

Carriers in Doped Semiconductors

	Majority Carriers	Minority Carriers
n-type	electrons	holes
p-type	holes	electrons

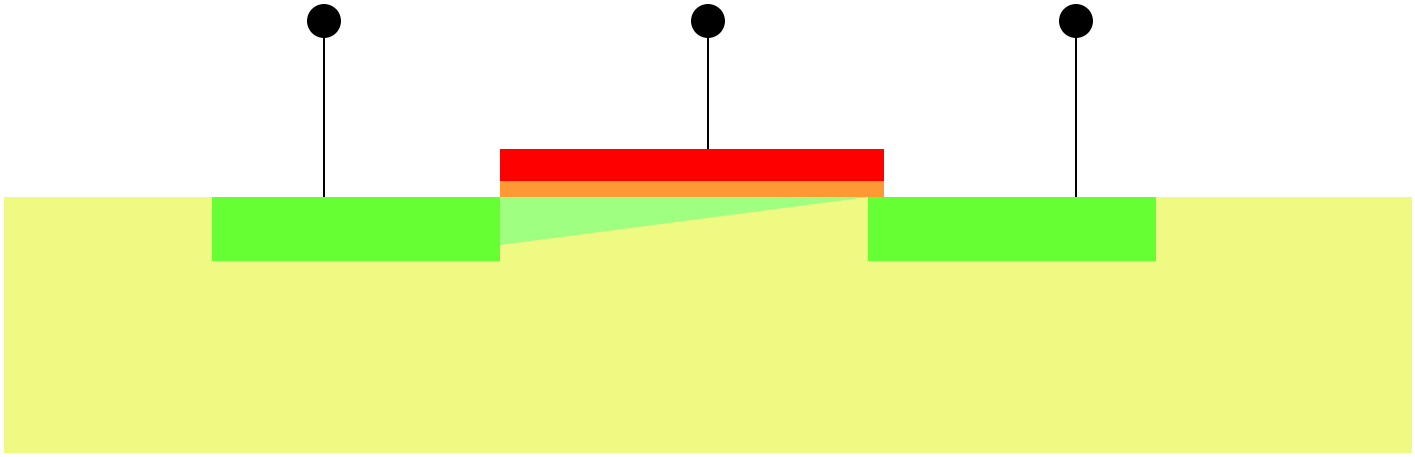
Carriers in MOS Transistors

Consider n-channel MOSFET

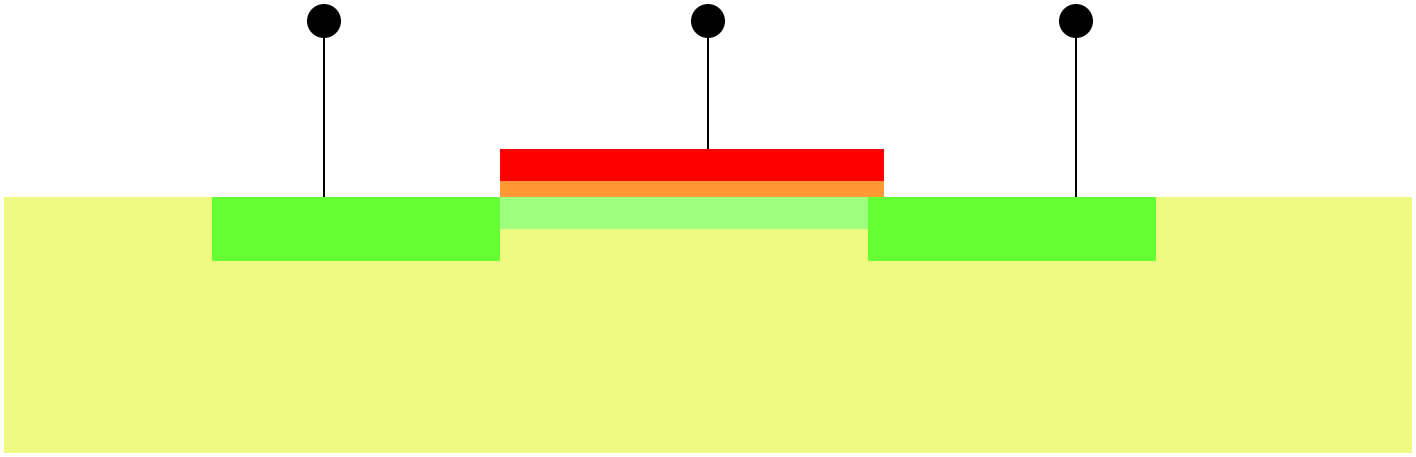


Carriers in MOS Transistors

Consider n-channel MOSFET



Saturation Region

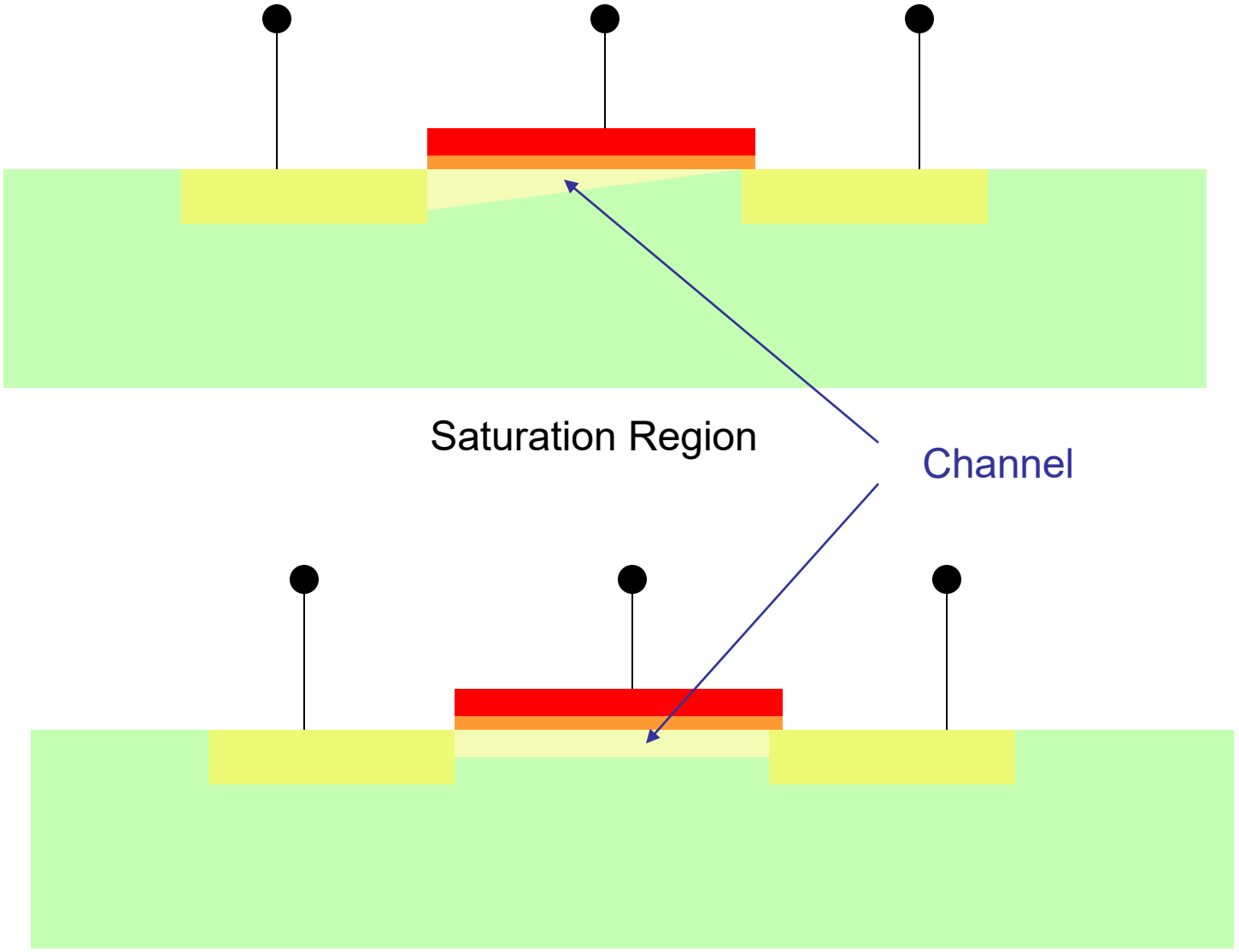


Triode Region

Carriers in electrically induced n-channel are electrons

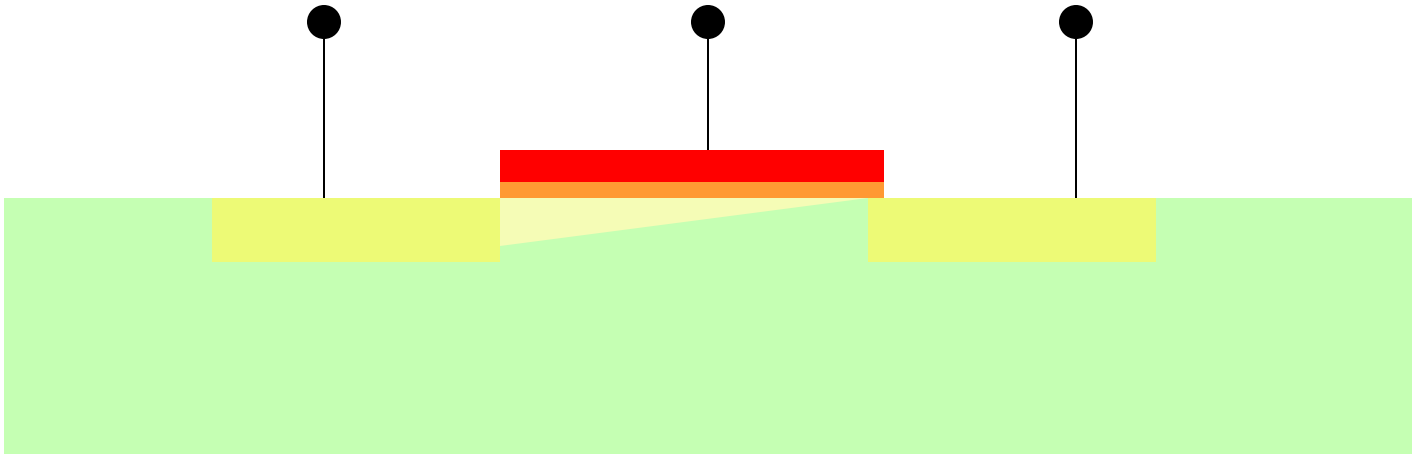
Carriers in MOS Transistors

Consider p-channel MOSFET

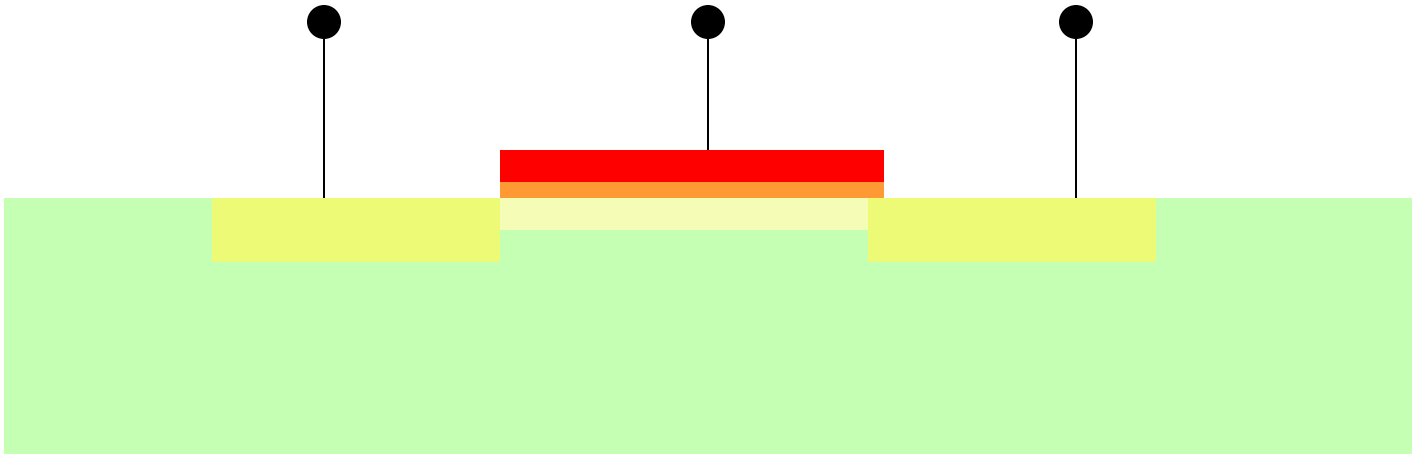


Carriers in MOS Transistors

Consider p-channel MOSFET



Saturation Region



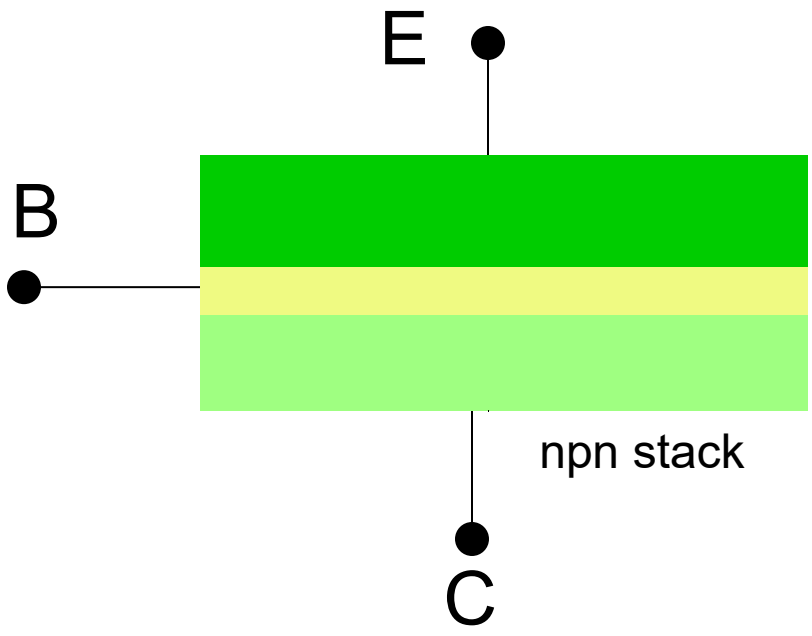
Triode Region

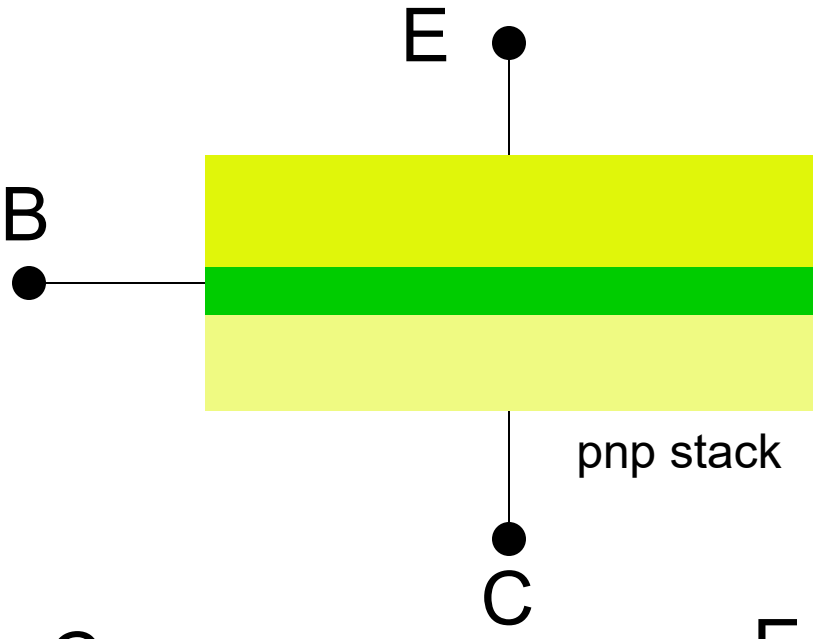
Carriers in electrically induced p-channel are holes

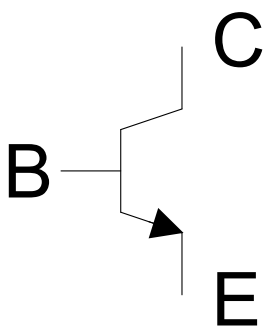
Carriers in MOS Transistors

Carriers in channel of MOS transistors are Majority carriers

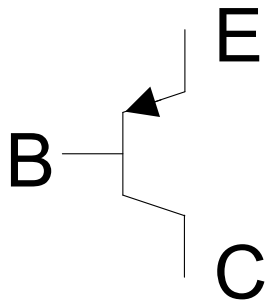
Bipolar Transistors







npn transistor

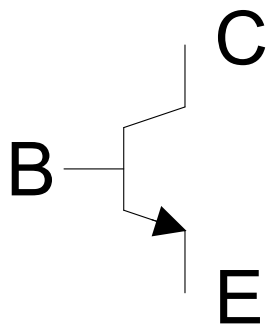


pnp transistor

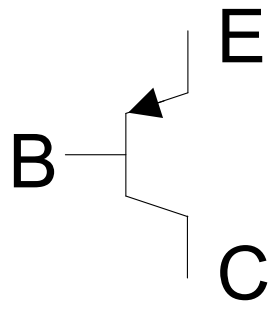
- **Bipolar Devices Show Basic Symmetry**
- **Electrical Properties not Symmetric**
- **Designation of C and E critical**

With proper doping and device sizing these form Bipolar Transistors

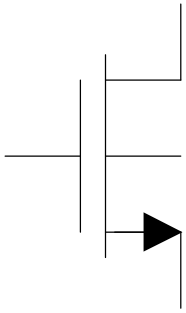
Bipolar Transistors



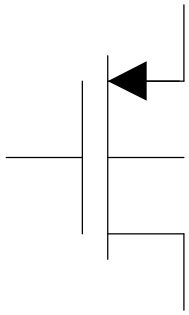
npn transistor



pnp transistor



n-channel MOSFET

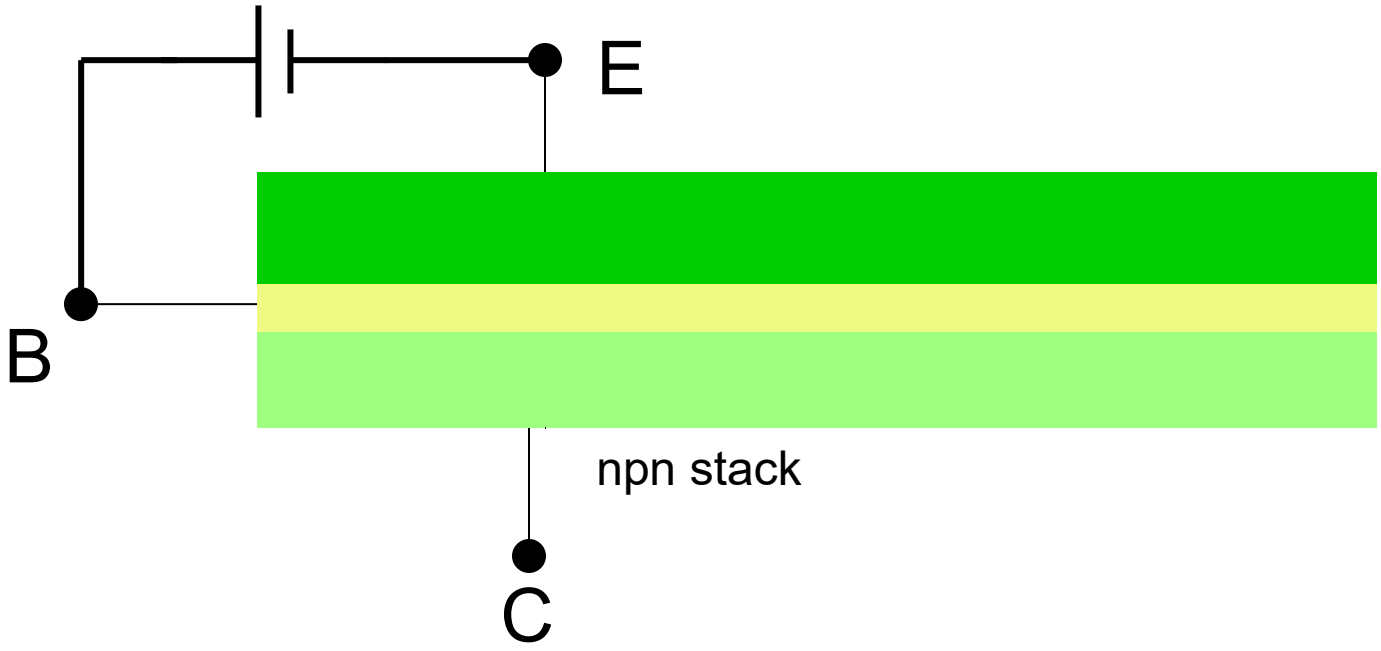


p-channel MOSFET

In contrast to a MOSFET which has 4 terminals, a BJT only has 3 terminals

Bipolar Operation

Consider npn transistor – Forward Active Operation



Under **forward BE bias** current flow into base and out of emitter

Current flow is governed by the diode equation

Carriers in emitter are electrons (majority carriers)

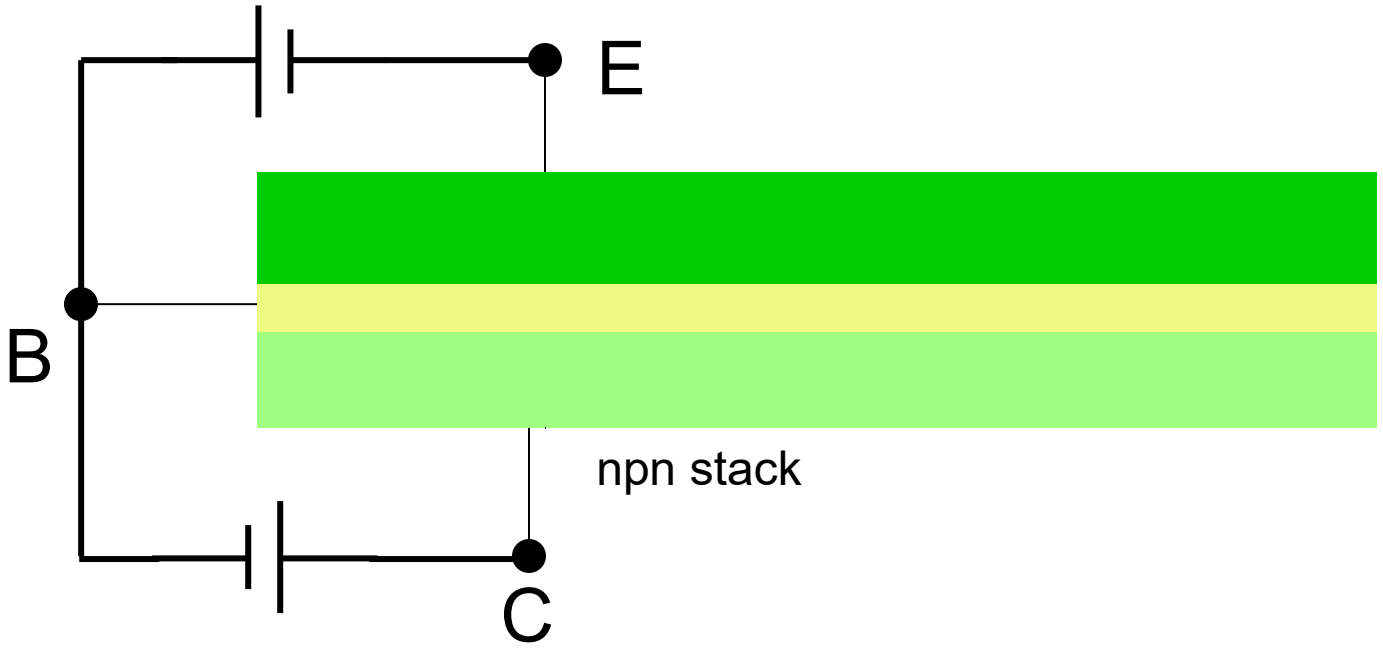
When electrons pass into the base they become minority carriers

Quickly recombine with holes to create holes in base region

Dominant current flow in base is holes (majority carriers)

Bipolar Operation

Consider npn transistor – Forward Active Operation



Under forward BE bias and reverse BC bias current flows into base **region**

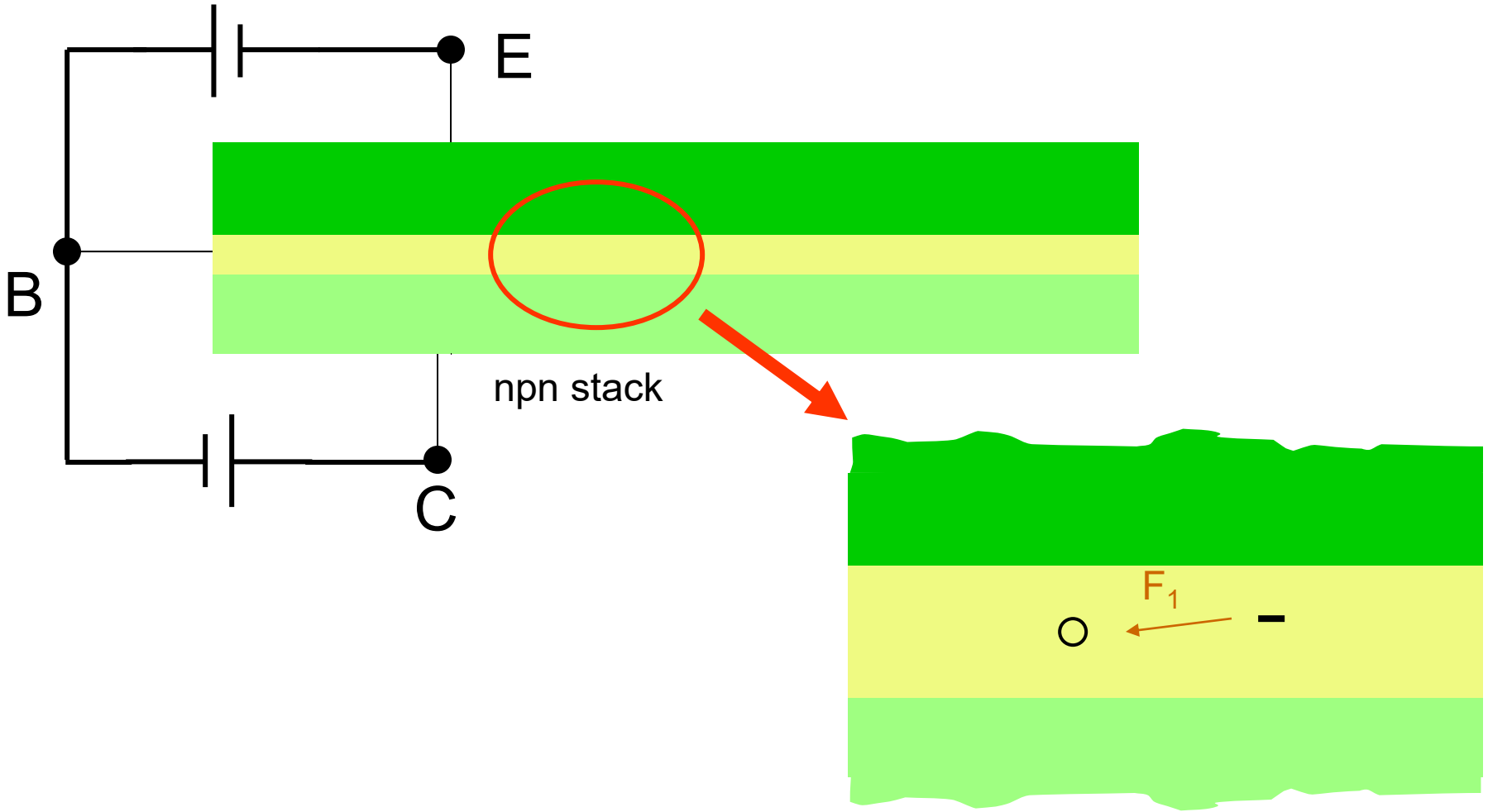
Carriers in emitter are electrons (majority carriers)

When electrons pass into the base they become minority carriers

When minority carriers are present in the base they can be attracted to collector

Bipolar Operation

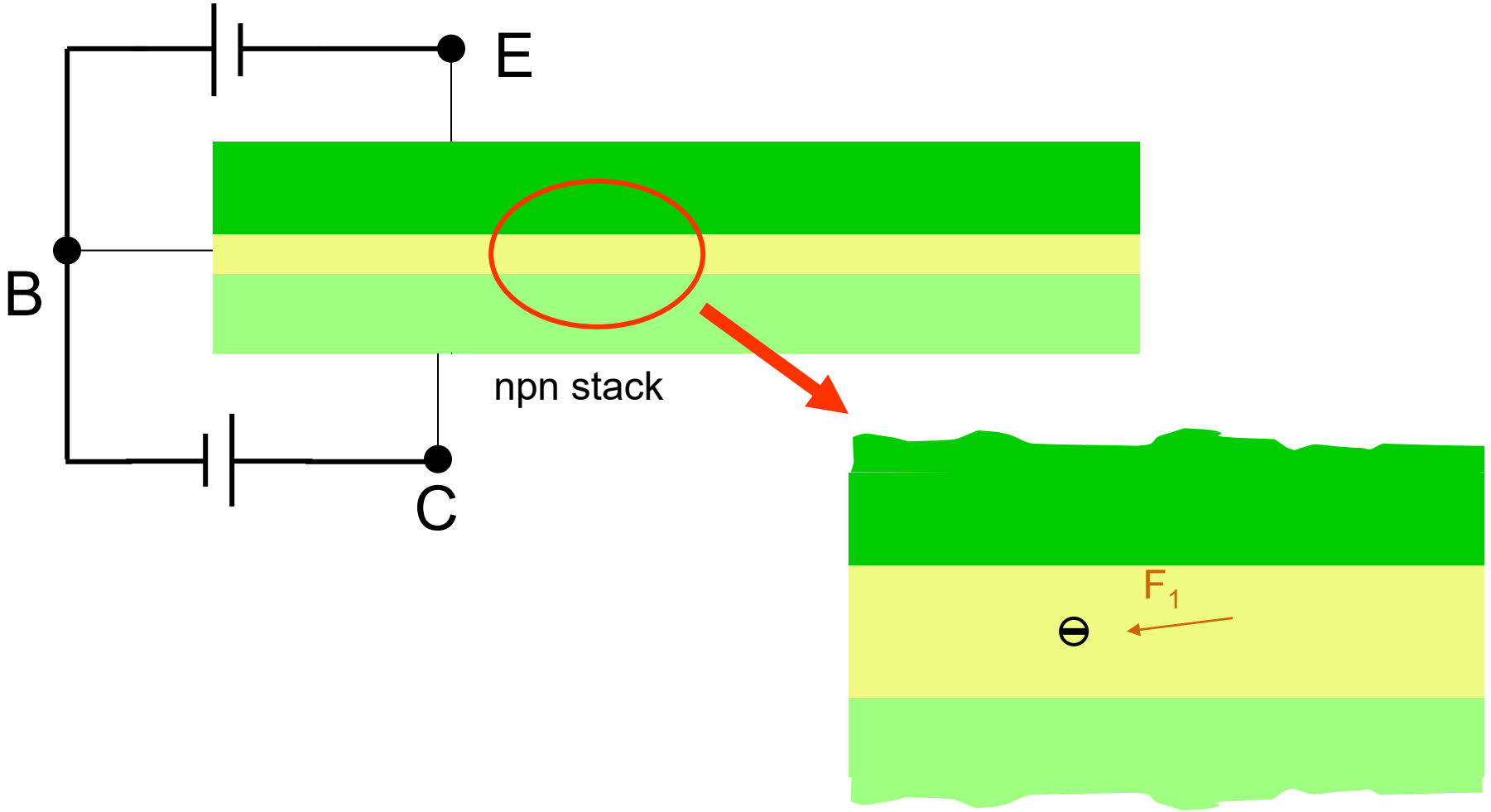
Consider npn transistor – Forward Active Operation



If no force on electron is applied by collector, electron will contribute to base current

Bipolar Operation

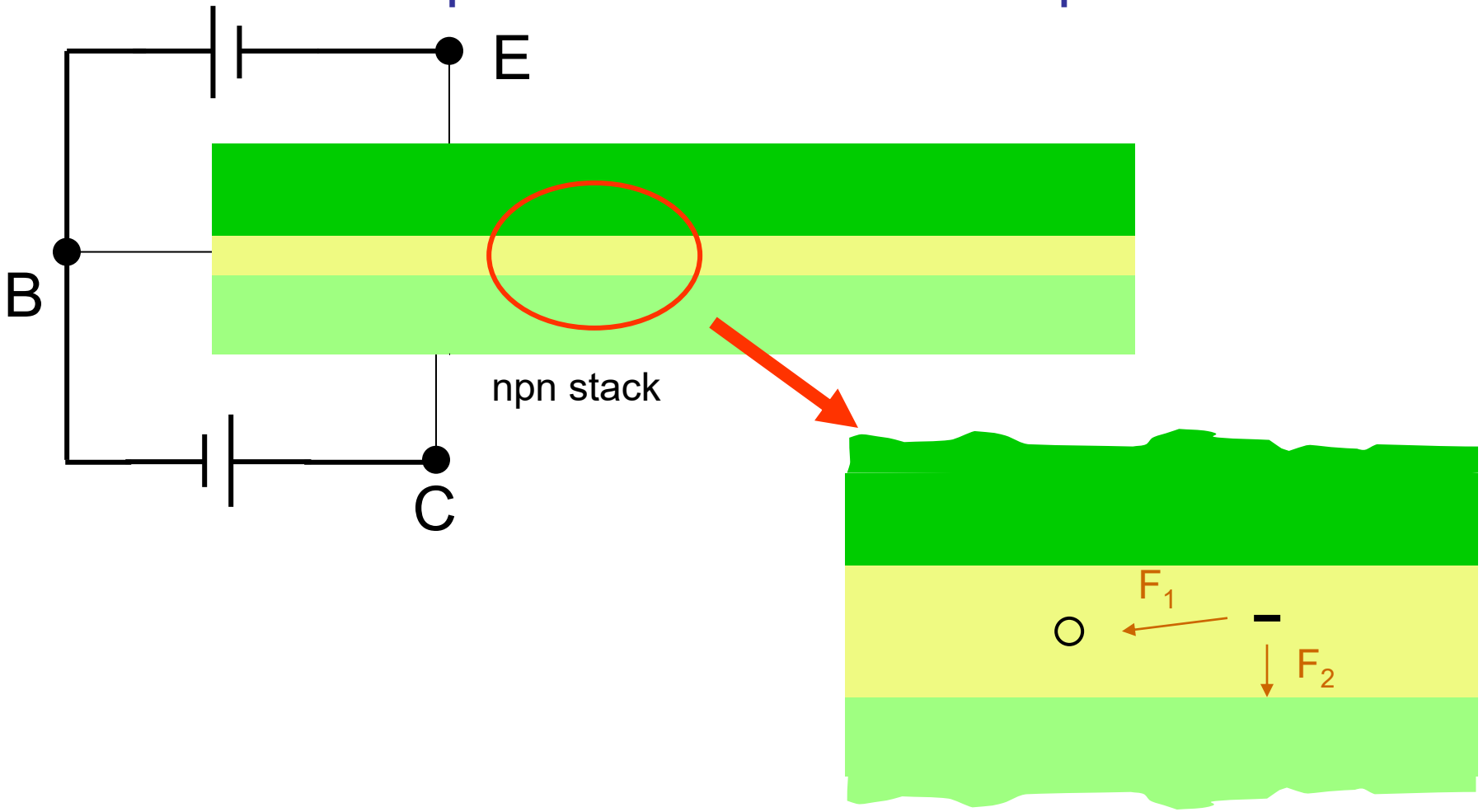
Consider npn transistor – Forward Active Operation



If no force on electron is applied by collector, electron will contribute to base current
Electron will recombine with a hole so dominant current flow in base will be by majority carriers

Bipolar Operation

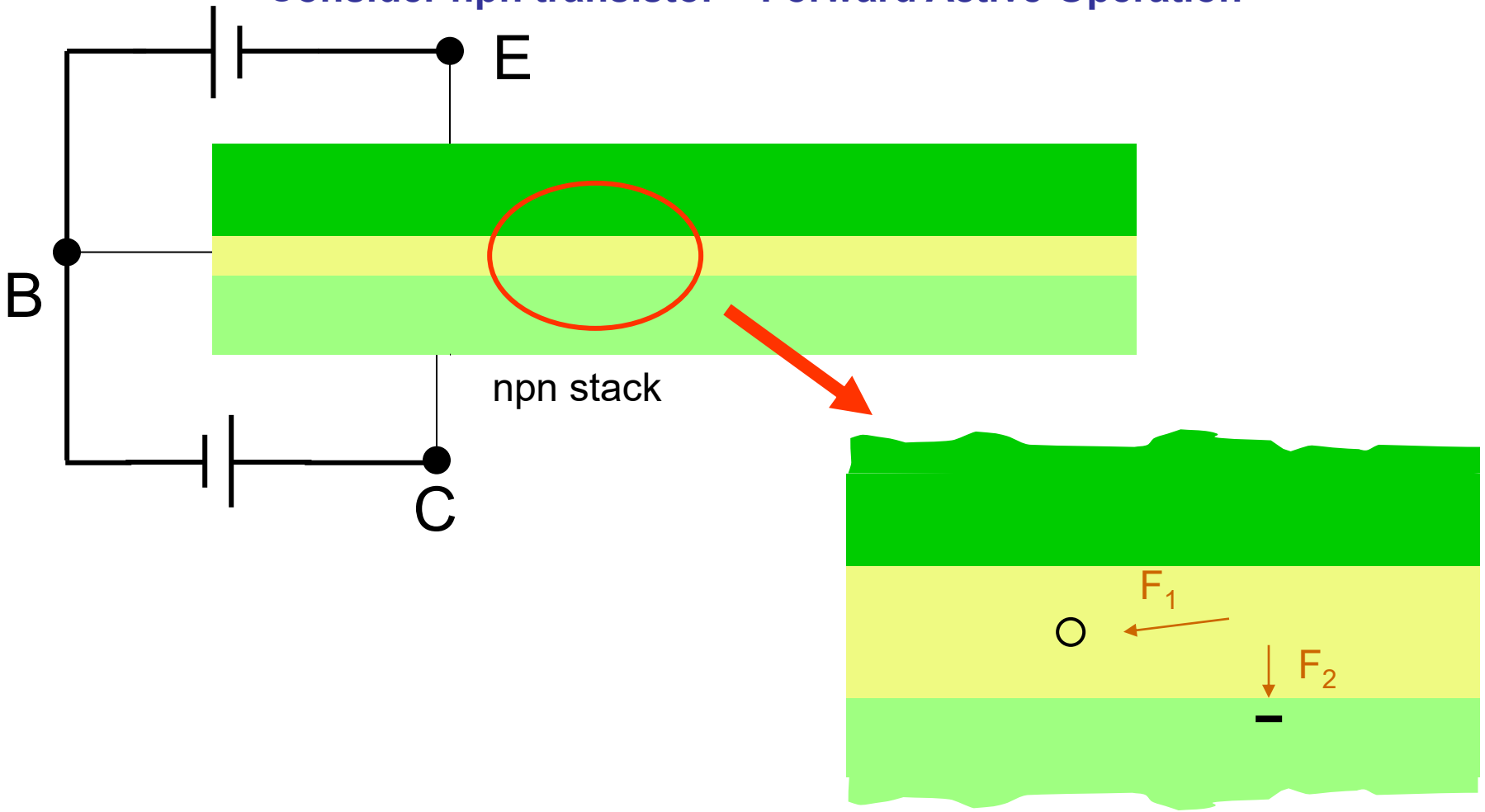
Consider npn transistor – Forward Active Operation



When minority carriers are present in the base they can be attracted to collector with reverse-bias of BC junction and can move across BC junction

Bipolar Operation

Consider npn transistor – Forward Active Operation

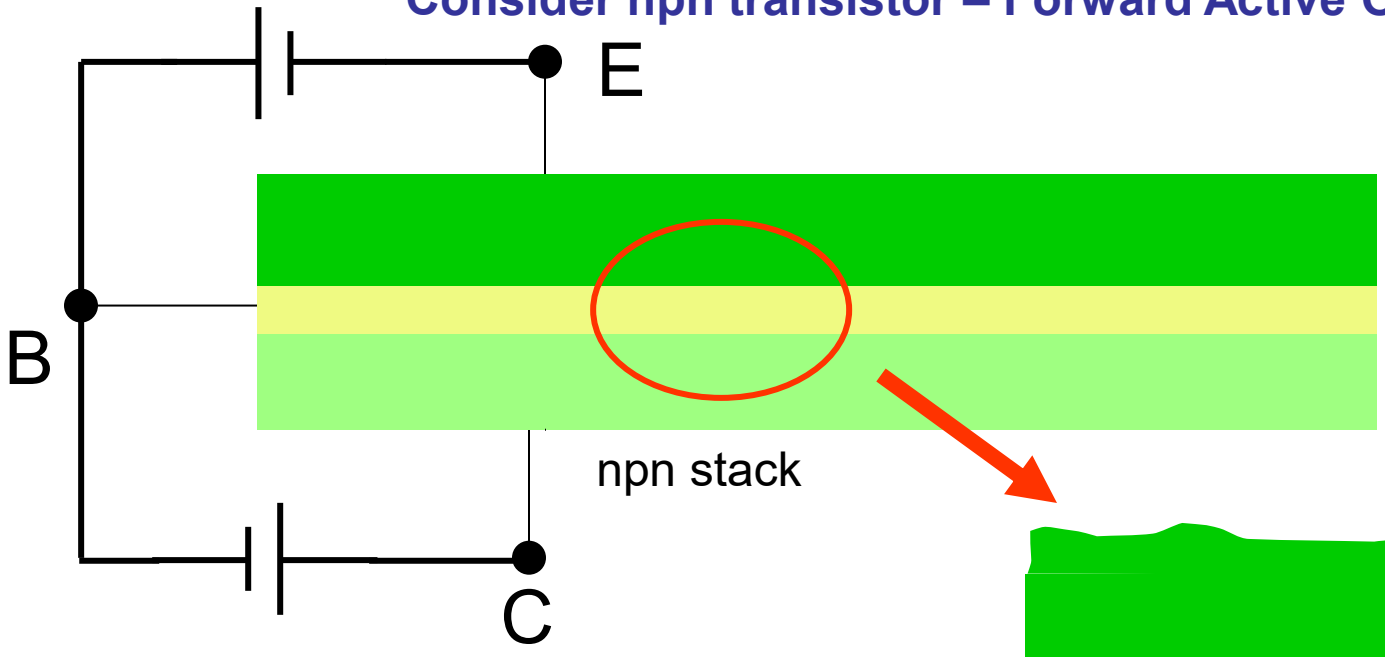


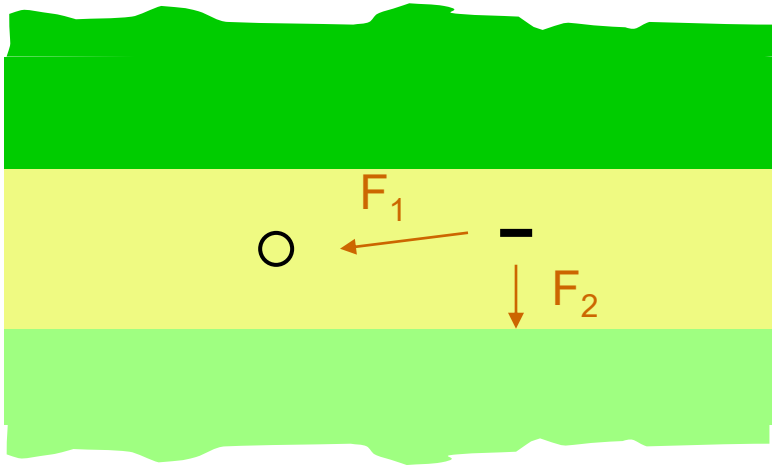
When minority carriers are present in the base they can be attracted to collector with reverse-bias of BC junction and can move across BC junction

Will contribute to collector current flow as majority carriers

Bipolar Operation

Consider npn transistor – Forward Active Operation

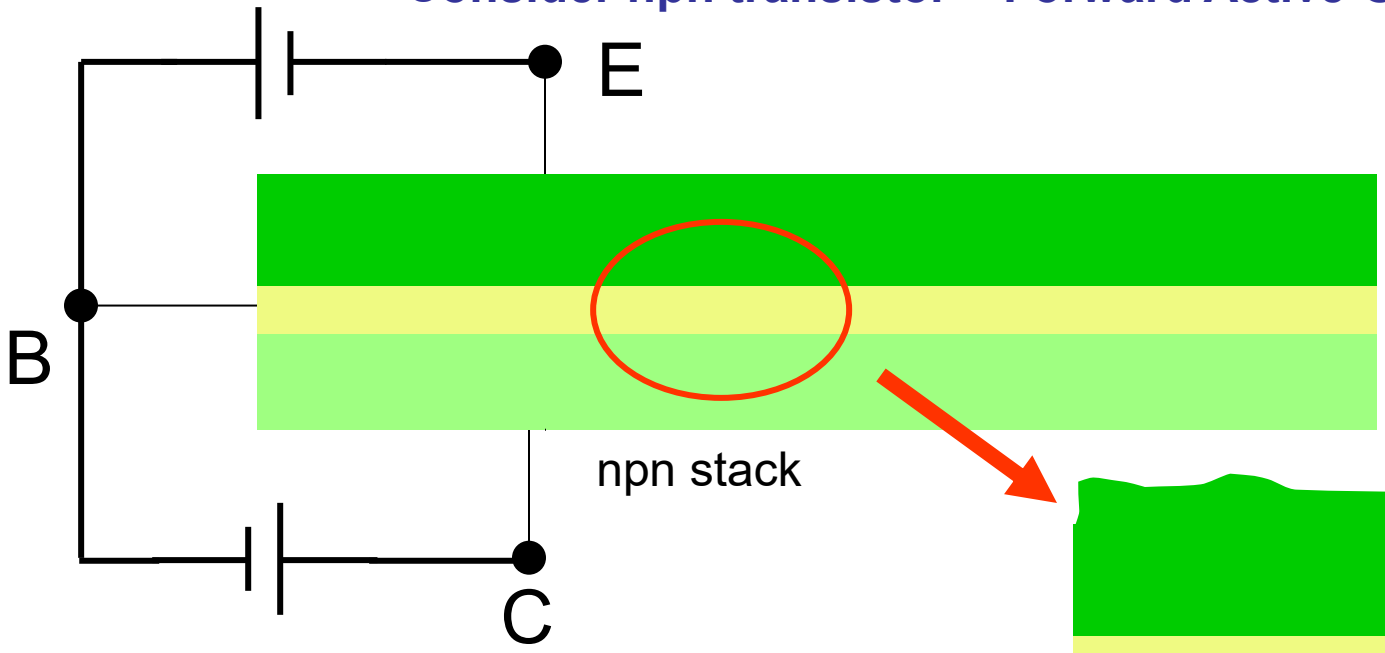


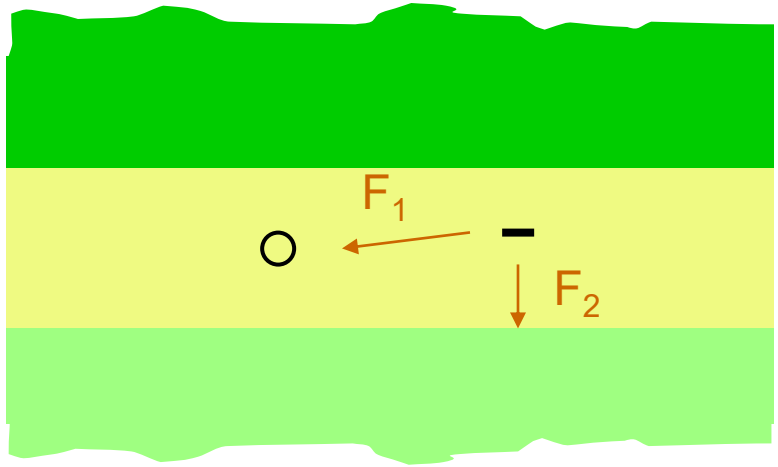


So, what will happen?

Bipolar Operation

Consider npn transistor – Forward Active Operation





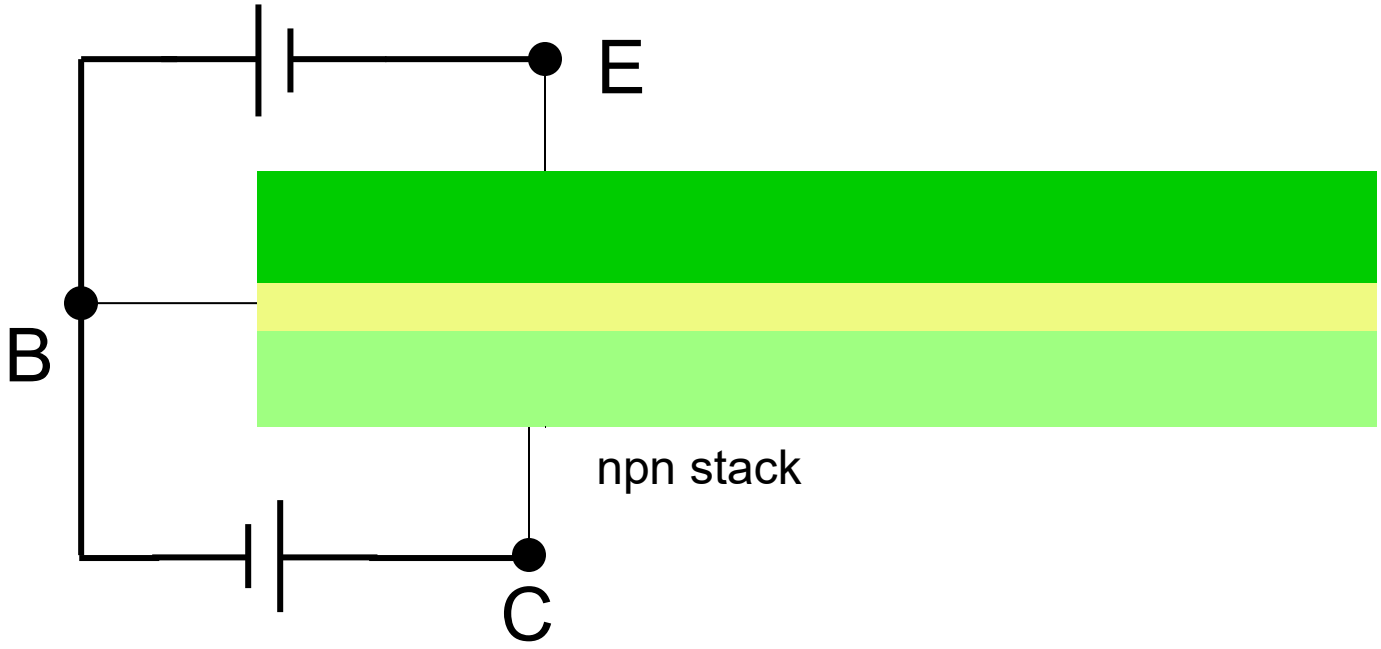
So, what will happen?

Some will recombine with holes and contribute to base current and some will be attracted across BC junction and contribute to collector

Size and thickness of base region and relative doping levels will play key role in percent of minority carriers injected into base contributing to collector current

Bipolar Operation

Consider npn transistor – Forward Active operation



Under forward BE bias and reverse BC bias current flows into base **region**

Carriers in emitter are electrons (majority carriers)

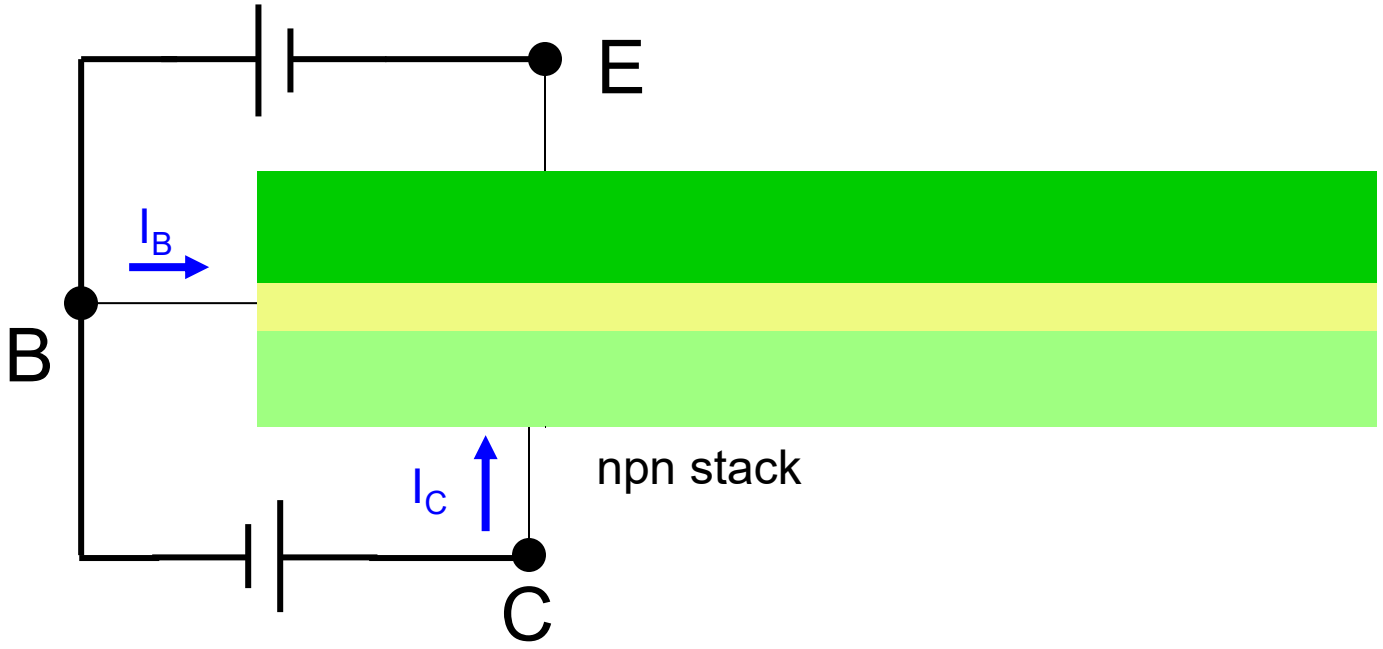
When electrons pass into the base they become minority carriers

When minority carriers are present in the base they can be attracted to collector

Minority carriers either recombine with holes and contribute to base current or are attracted into collector region and contribute to collector current

Bipolar Operation

Consider npn transistor – Forward Active operation



Minority carriers either recombine with holes and contribute to base current or are attracted into collector region and contribute to collector current

If most of the minority carriers are attracted to collector, $|I_c| \simeq |I_E|$

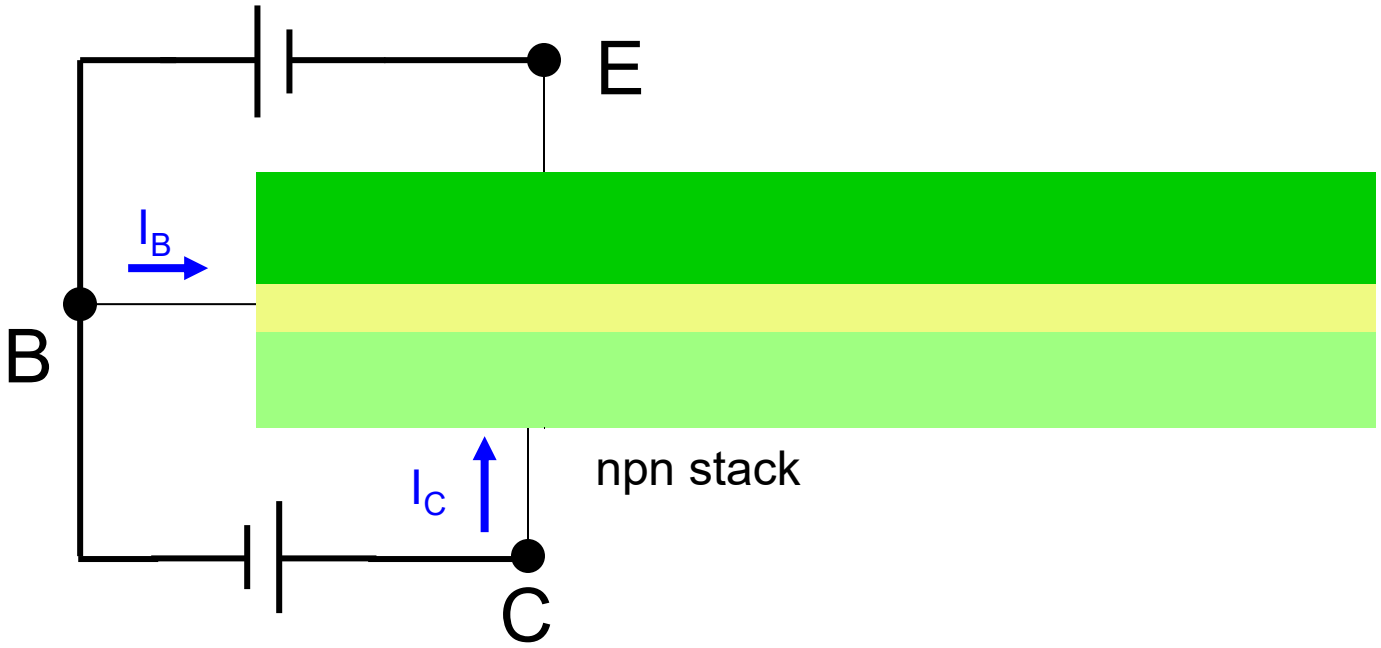
Thus $I_B << I_C$

Implications of this observation?

If input to device is I_B and output is I_C, the BJT will behave as a current amplifier with large current gain !! This was the key observation by Bell Labs in 1948 !!

Bipolar Operation

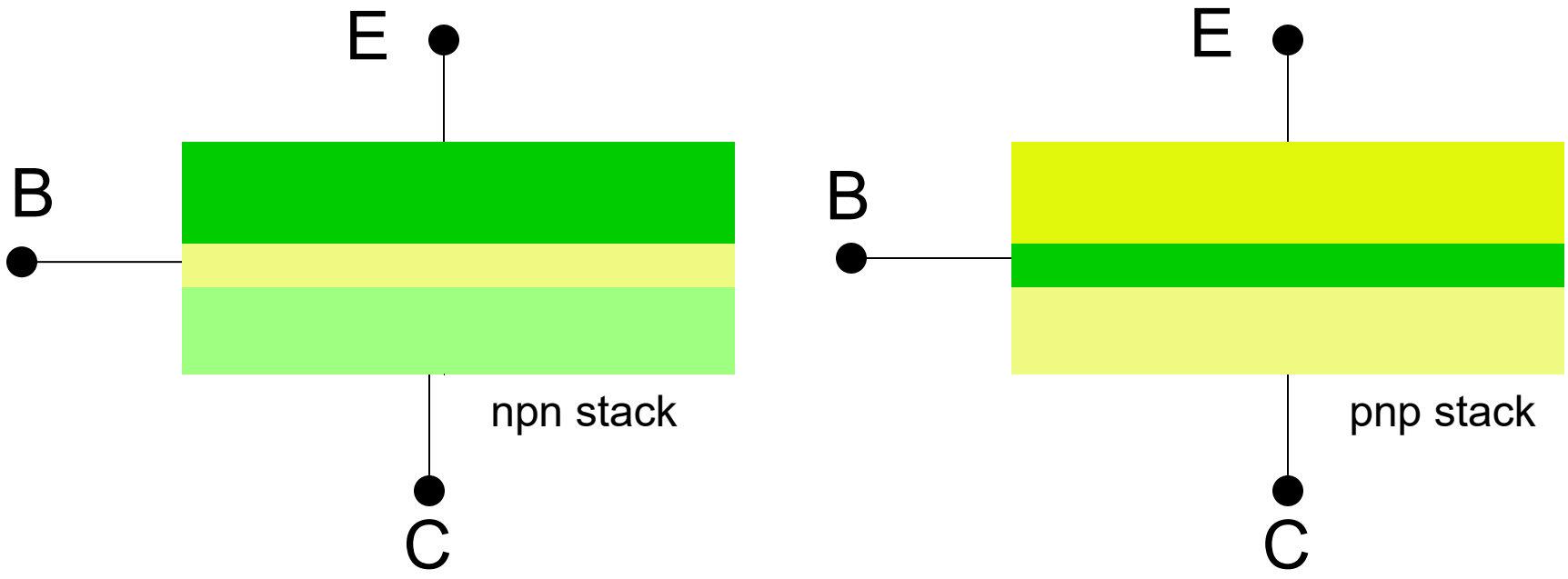
Consider npn transistor - Forward Active Operation



Under forward BE bias and reverse BC bias current flows into base **region**

- Efficiency at which minority carriers injected into base region and contribute to collector current is termed α
- α is always less than 1 but for a good transistor, it is very close to 1
- For good transistors .99 < α < .999
- Making the base region very thin makes α large

Bipolar Transistors

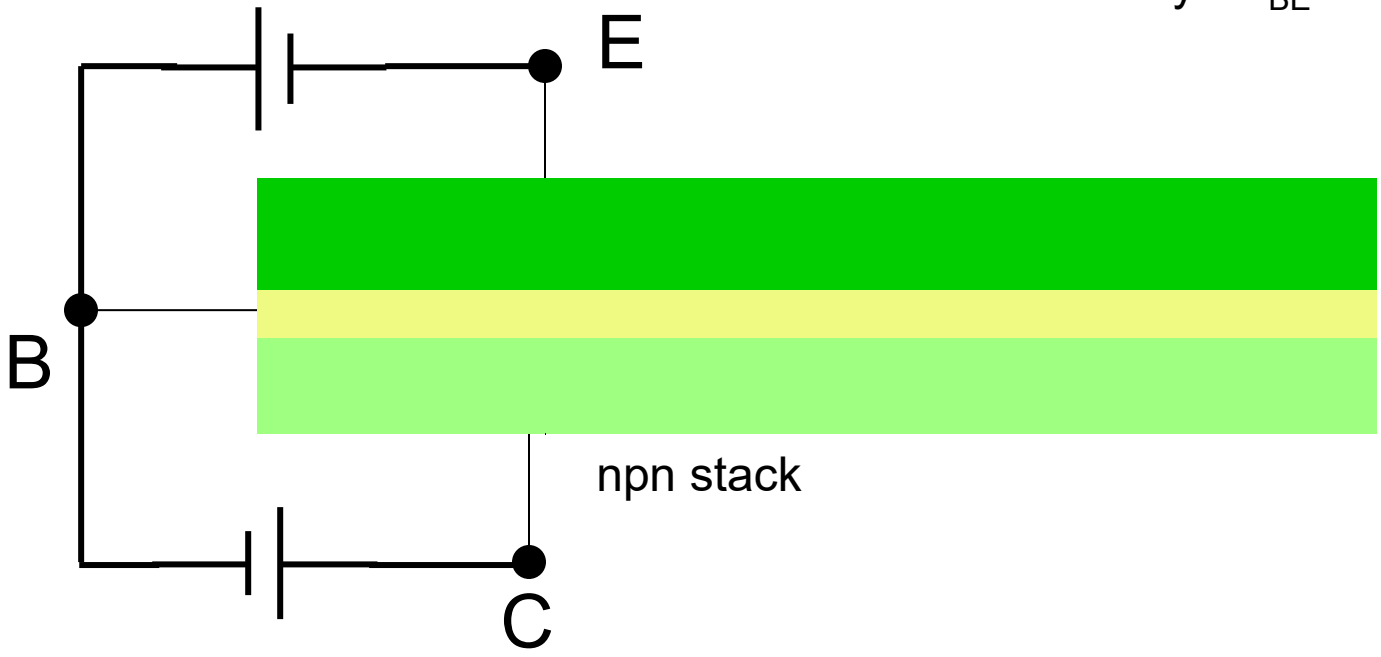


- principle of operation of pnp and npn transistors are the same
- minority carriers in base of pnp are holes
- npn usually have modestly superior properties because mobility of electrons is larger than mobility of holes

Bipolar Operation

Consider npn transistor – Forward Active Operation

tentatively: $V_{BE}>0.4$ $V_{BC}<0.4$

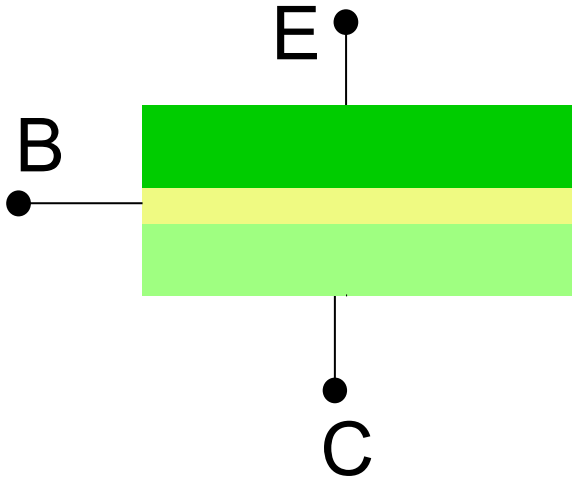


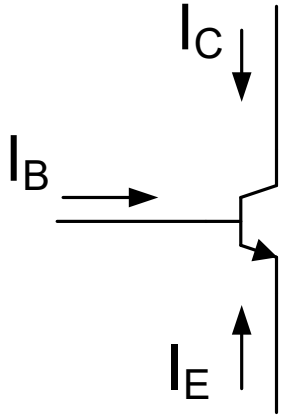
In contrast to MOS devices where current flow in channel is by majority carriers, current flow in the critical base region of bipolar transistors is by minority carriers

Bipolar Operation

Consider npn transistor – Forward Active Operation

tentatively: $V_{BE}>0.4$ $V_{BC}<0.4$





$$I_C + I_B = -I_E$$

$$I_C = -\alpha I_E$$

$$I_C = \frac{\alpha}{1-\alpha} I_B$$

$$\beta \overset{defn}{=} \frac{\alpha}{1-\alpha}$$

$$I_C = \beta I_B$$

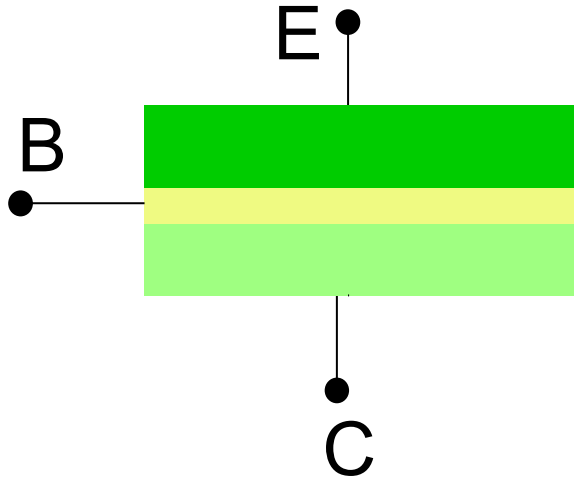
β is typically very large

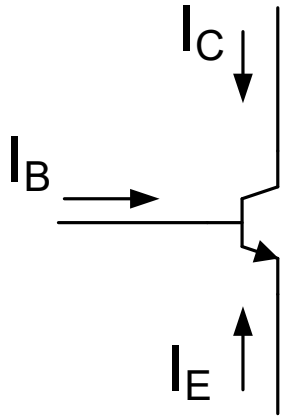
often 50<β<999

Bipolar Operation

Consider npn transistor – Forward Active Operation

tentatively: $V_{BE}>0.4$ $V_{BC}<0.4$





$$I_C = \beta I_B$$

β is typically very large

Bipolar transistor can be thought of as current amplifier with a large current gain

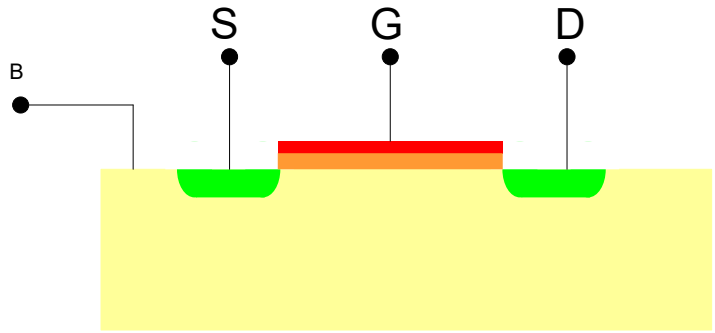
In contrast, MOS transistor is inherently a tramsconductance amplifier

Current flow in base is governed by the diode equation $I_B = \tilde{I}_S e^{\frac{V_{BE}}{V_t}}$

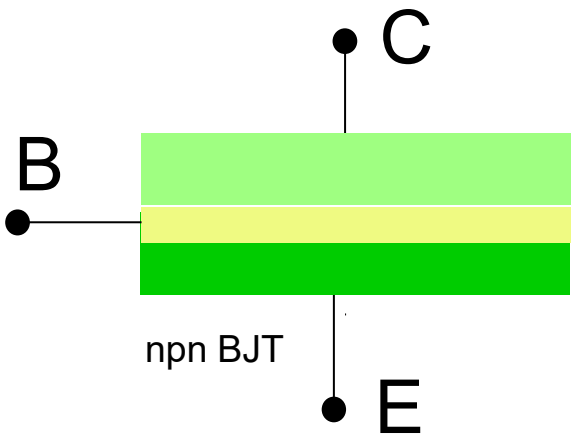
Collector current thus varies exponentially with V_{BE} $I_C = \beta \tilde{I}_S e^{\frac{V_{BE}}{V_t}}$

Preliminary Comparison of MOSFET and BJT

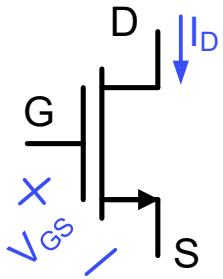
(Saturation vs Forward Active)

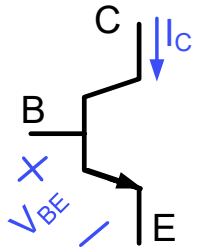


n-channel MOSFET



npn BJT





$$I_D = \frac{\mu C_{OX} W}{2L}\left(V_{GS} - V_{TH}\right)^2$$

$$I_C = \beta \tilde{I}_S e^{\frac{V_{BE}}{V_t}}$$

I_D independent of V_{DS} ⟷ I_C independent of V_{CE}

- The BJT I/O relationship is exponential in contrast to square-law for MOSFET
- Provides a very large “gain” for the BJT (assuming input is voltage and output is current)
- This property is very useful for many applications

Stay Safe and Stay Healthy !

End of Lecture 19